Energy-Delay Performance of Capacitive Threshold Logic (CTL) Circuits for Threshold Detection

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METU NORTHERN CYPRUS CAMPUS

IEEE

Outline

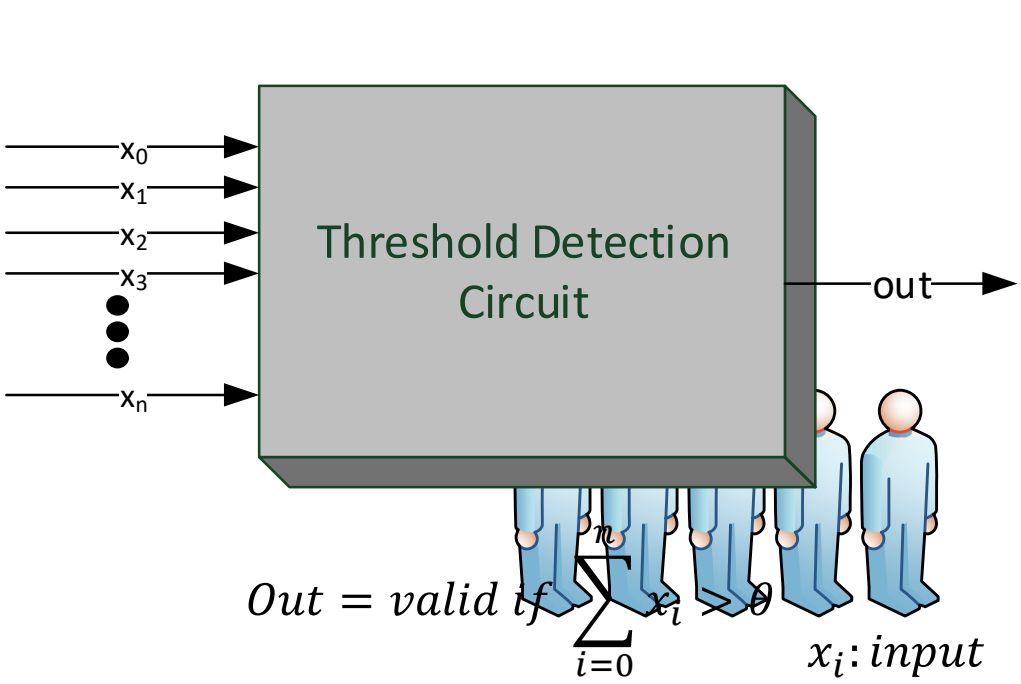
- Introduction: Threshold Detection
- Motivation
- Digital & Analog TL Solutions
- Complexity
- Implementation & Simulation
- Results
- Conclusion & Future Work

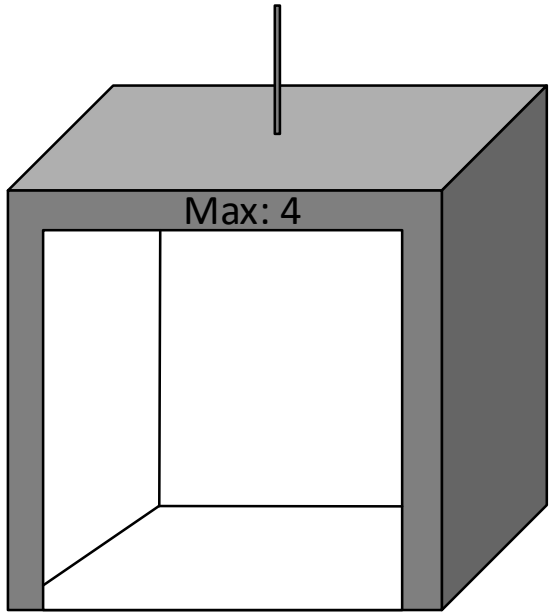
Introduction

- Recent focus on energy efficiency
  - Diminishing ready-to-use energy resources
  - Pollutant byproducts of conventional energy resources
  - Shrinking computing platforms (e.g. smartphones)
- Energy efficient computing
  - 'Performance first' approach in the past
  - Mobile computing
  - Concerning battery life

Threshold Detection

- A system that detects when number of active inputs exceeds a threshold value





Area of use & Potential Impact

- Arithmetic processing
  - e.g. multiplication (computing)
- Neural networks
  - e.g. freeway incident detections
  - e.g. biological neuron stimulus simulations

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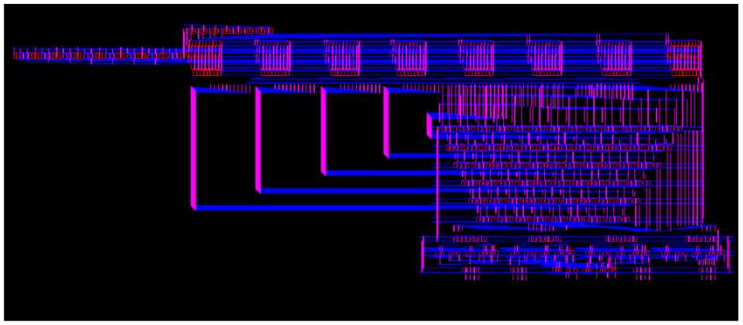

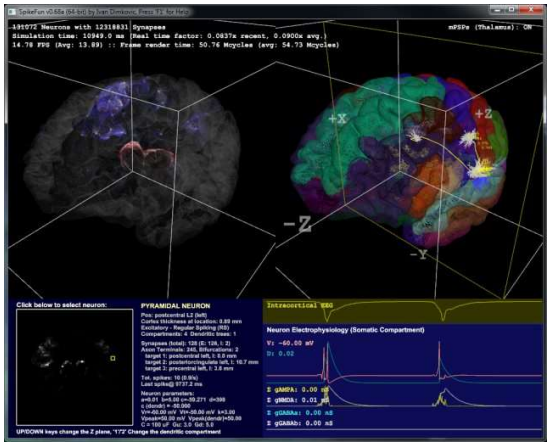

Any improvement on threshold logic would have a vast impact on the topologies that employ it!

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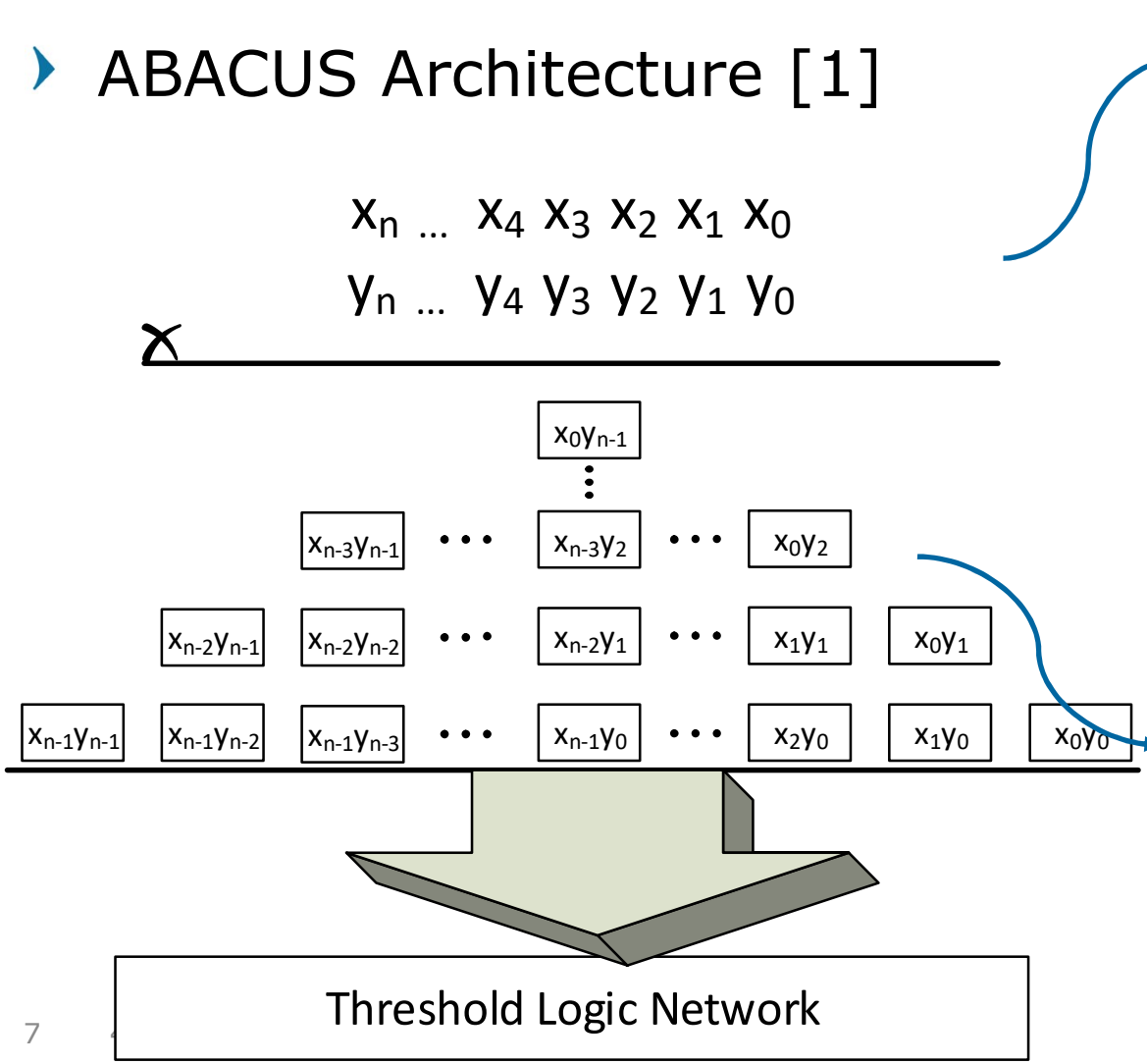
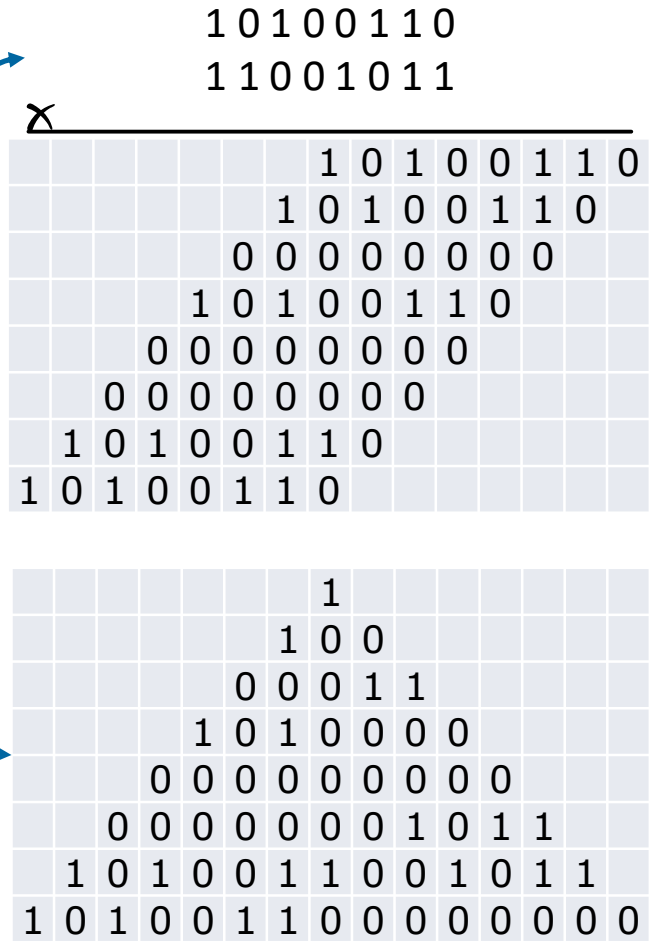
Motivation - I

- ABACUS Architecture [1]

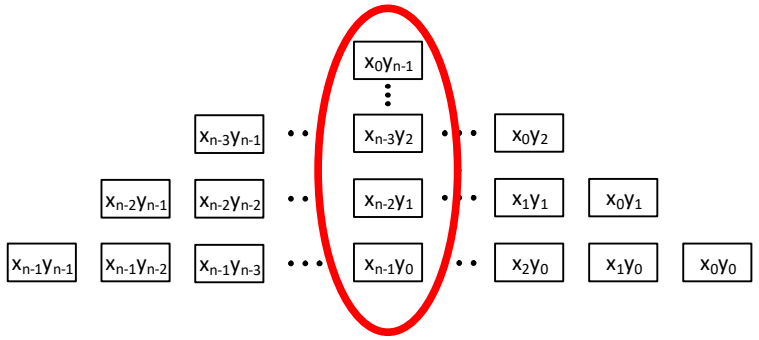




Motivation - II

Architectural assesment of ABACUS multiplier with respect to other multipliers, Didem Gürdür (2013, M.Sc. Thesis, SEES) [2]

- Energy-delay product (EDP) of ABACUS was compared to
  - Wallace tree multiplier
  - Carry-Save array multiplier
  - Ripple-carry adder multiplier



- ABACUS is better than all except Wallace
  - ~20% performance improvement is needed at the mid-column compression

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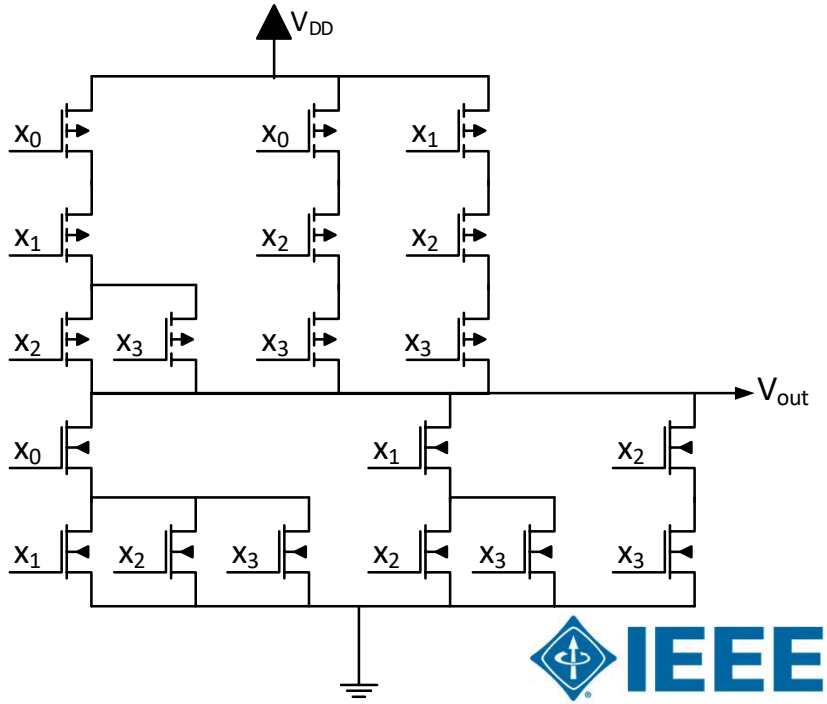
Digital Threshold Detection Methods - I

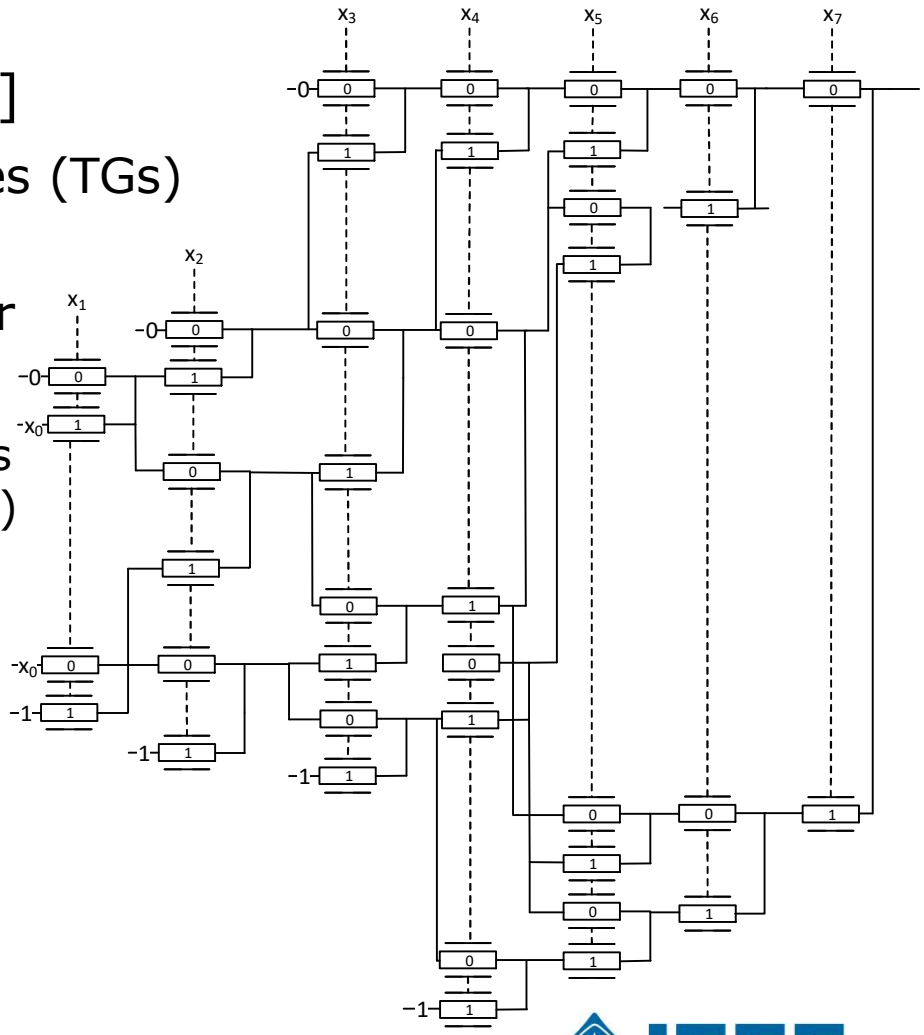
- Compound CMOS based TL [3]
  - 90 nm technology was used
  - Fan-in issues as inputs/threshold gets larger
    - Max MOSFET in series: 4 (performance issues)
  - Figure: A 2/4 CMOS based TL



Digital Threshold Detection Methods - II

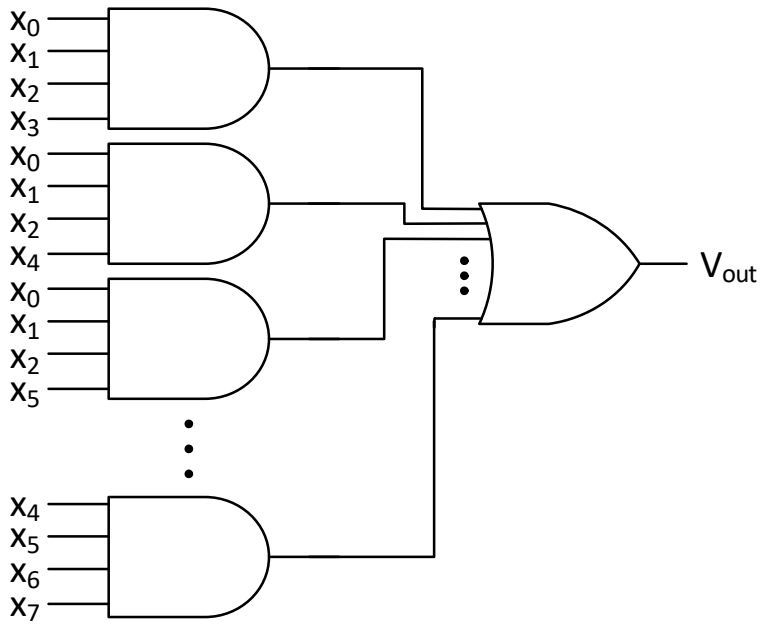
- Transmission Gate based TL [4]
  - Inputs control transmission gates (TGs)
  - Modular approach was used to minimize circuit area, and power
    - No effect on delay
    - i.e. 40 TGs instead of ~250, saves 84% area (and power accordingly)

Figure: A 4/8 XTL



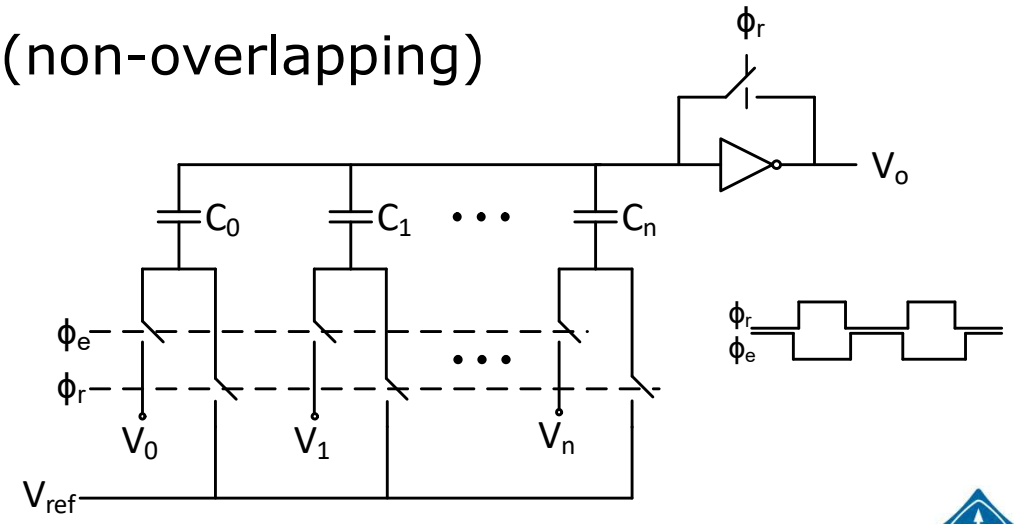
Digital Threshold Detection Methods - III

- Logic Gate level TL
  - Gate-Level logic design
  - Threshold combinations of all n inputs
  - Fan-in issues encountered



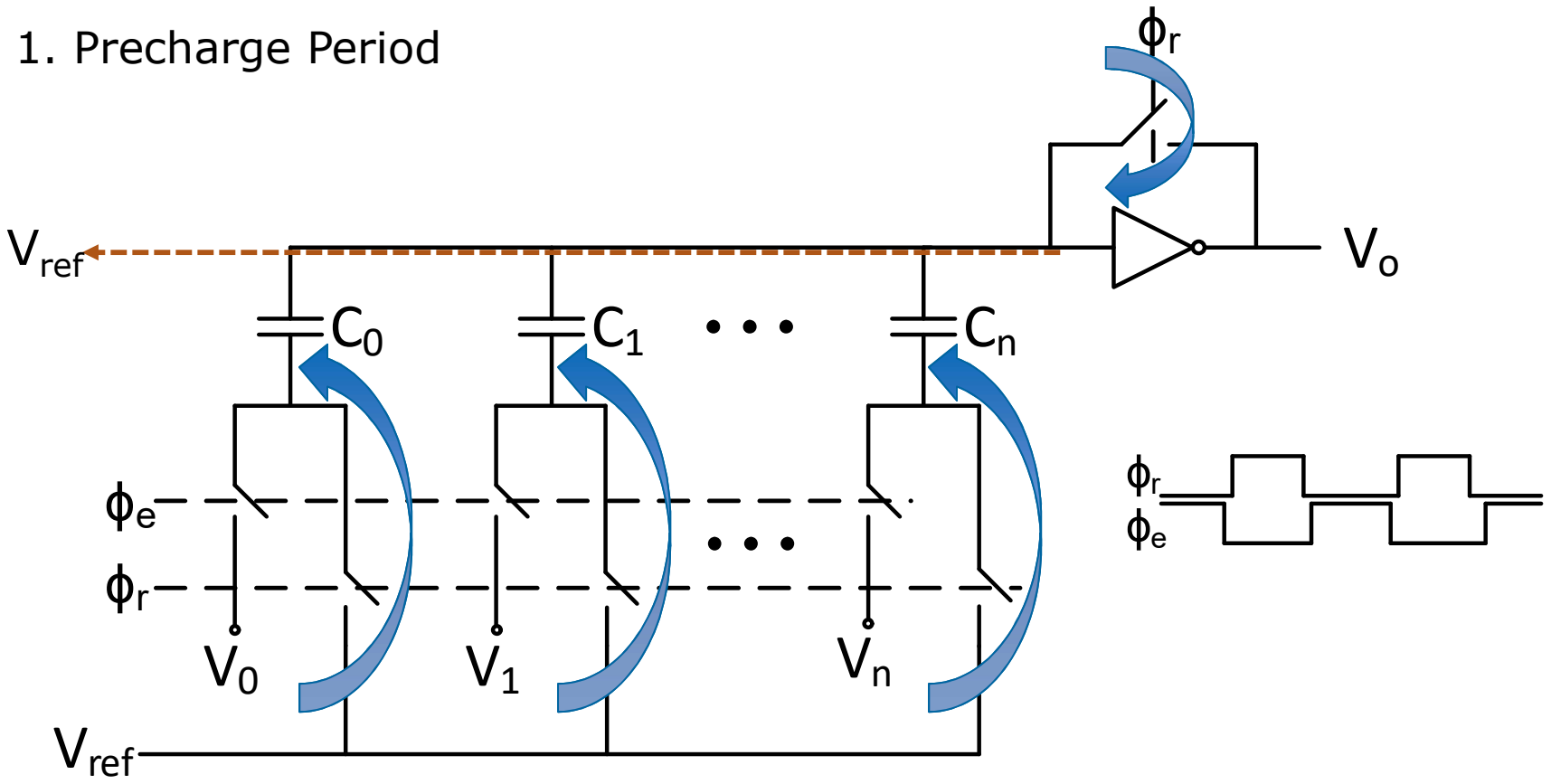
Analog Threshold Detection Methods - I

- Capacitive TL [5,6]
  - Regular design
  - Threshold/input vs. circuit complexity is not an issue
    - e.g. directly proportional to # of inputs
    - e.g. threshold has no effect on it
  - Control clocks (non-overlapping)



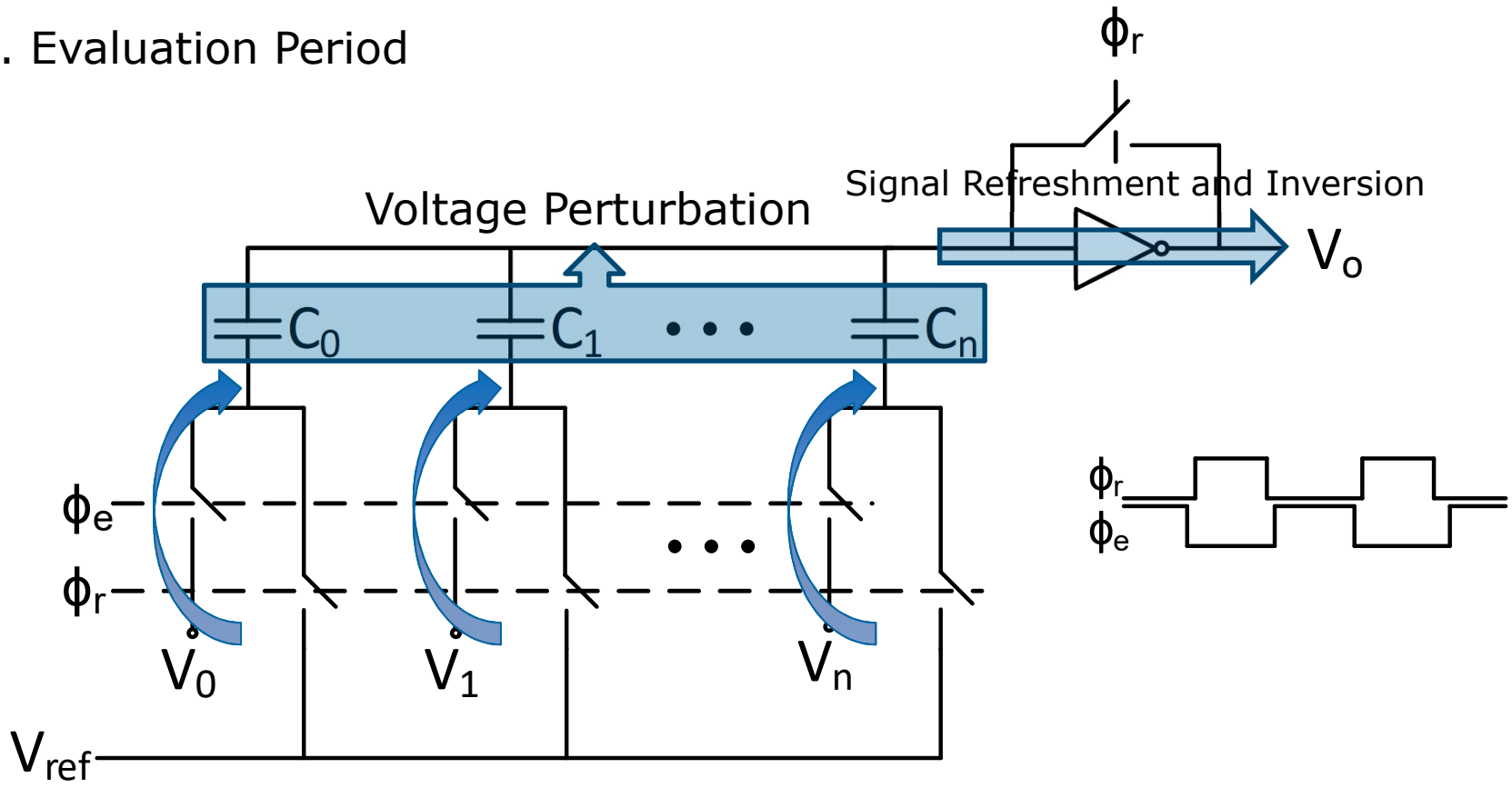
Capacitive TL

1. Precharge Period



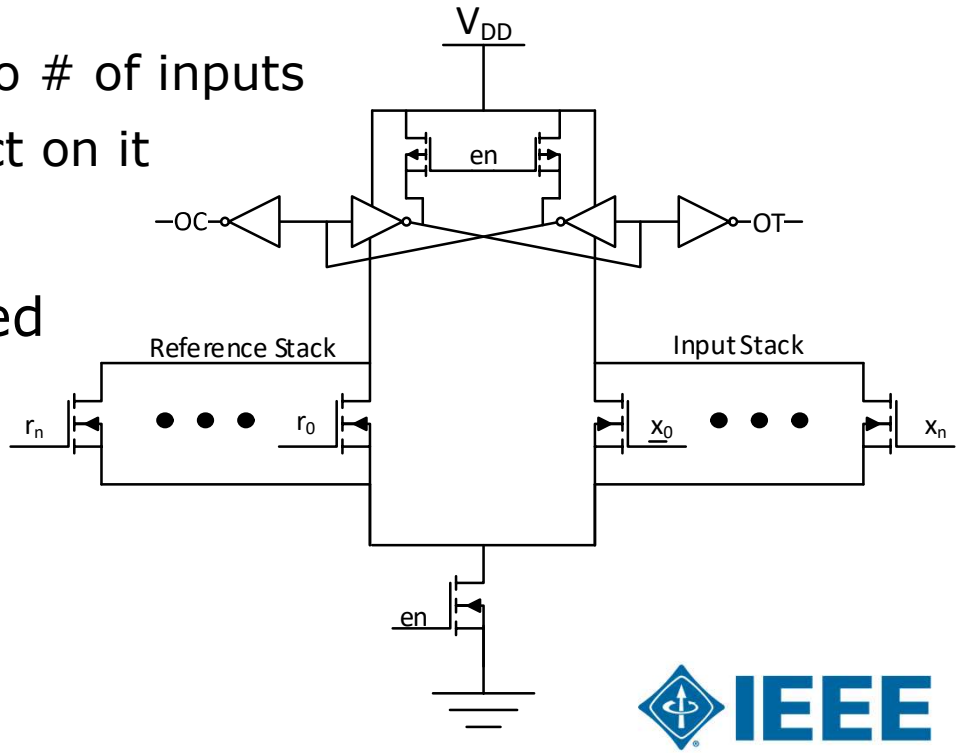
Capacitive TL

2. Evaluation Period



Analog Threshold Detection Methods - II

- Differential TL [7]
  - Regular design
  - Threshold/input vs. circuit complexity is not an issue
    - e.g. directly proportional to # of inputs
    - e.g. threshold has no effect on it
  - Control clock
  - Reference nodes connected either to V_{DD} or GND
  - Current is compared
  - Sensitive design



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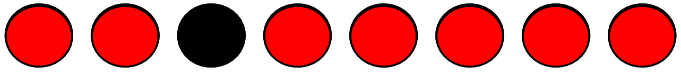
Circuit complexity vs. power - I

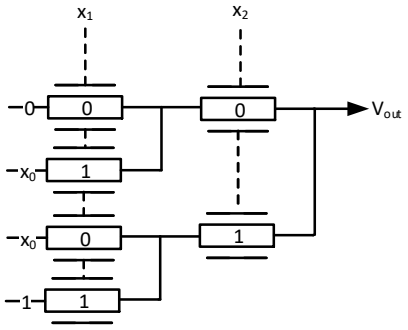
- With respect to:
  - Number of inputs
  - Threshold value

Demonstration:
Red: Active **Black: Non-active**

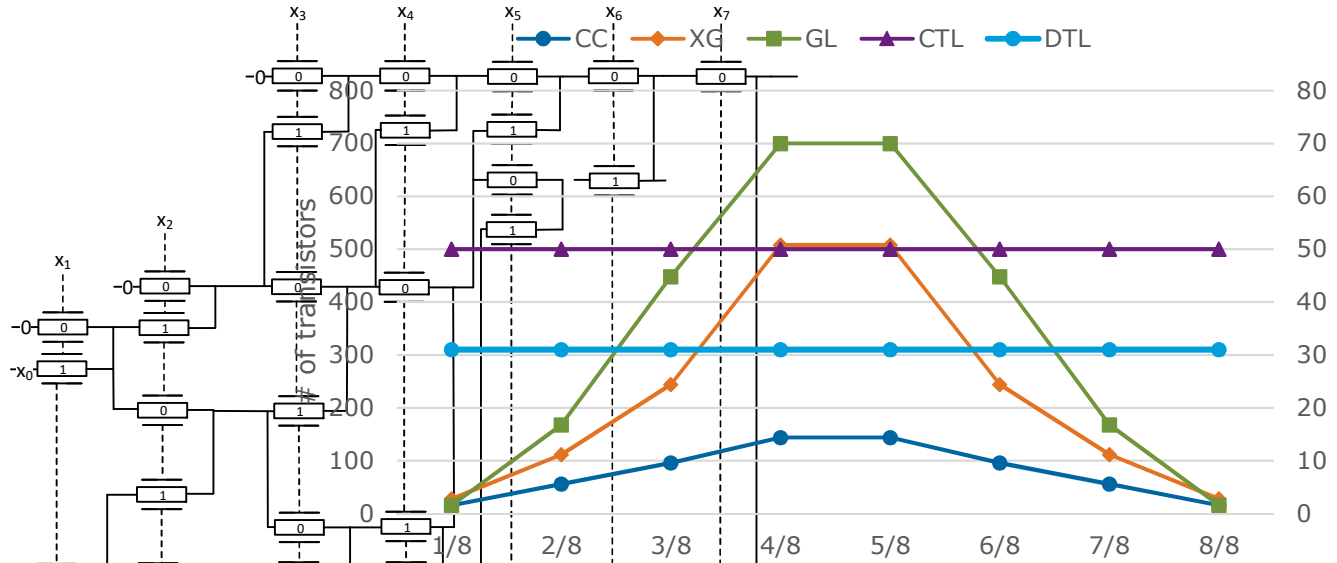


- Larger the circuit, larger the
  - Dynamic power: switching networks
  - Static power: idle networks
  - Elapsed time

Circuit complexity vs. power - II



2/3 Transmission Gate TL



Threshold Value vs. Circuit Complexity

Easier to detect 1/n & n/n
Gets more difficult to catch through (n/2)/n

4/8 Transmission Gate TL

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Implementation & Simulation

- Implemented in 90 nm CMOS technology
  - Minimum size for all designs
  - Relative trends w.r.t. # of inputs are emphasized more than absolute values
- Simulated to measure
  - Energy
  - Delay

  } Energy-Delay Product (EDP)
- Digital (CMOS-based) solutions are synchronized (clocked) for a fair comparison
- 2/4, 3/6, 4/8 TLs are analyzed
  - CTL currently does not support inputs more than ~10
  - 3/6 is presented to emphasize the trend between 2/4 & 4/8

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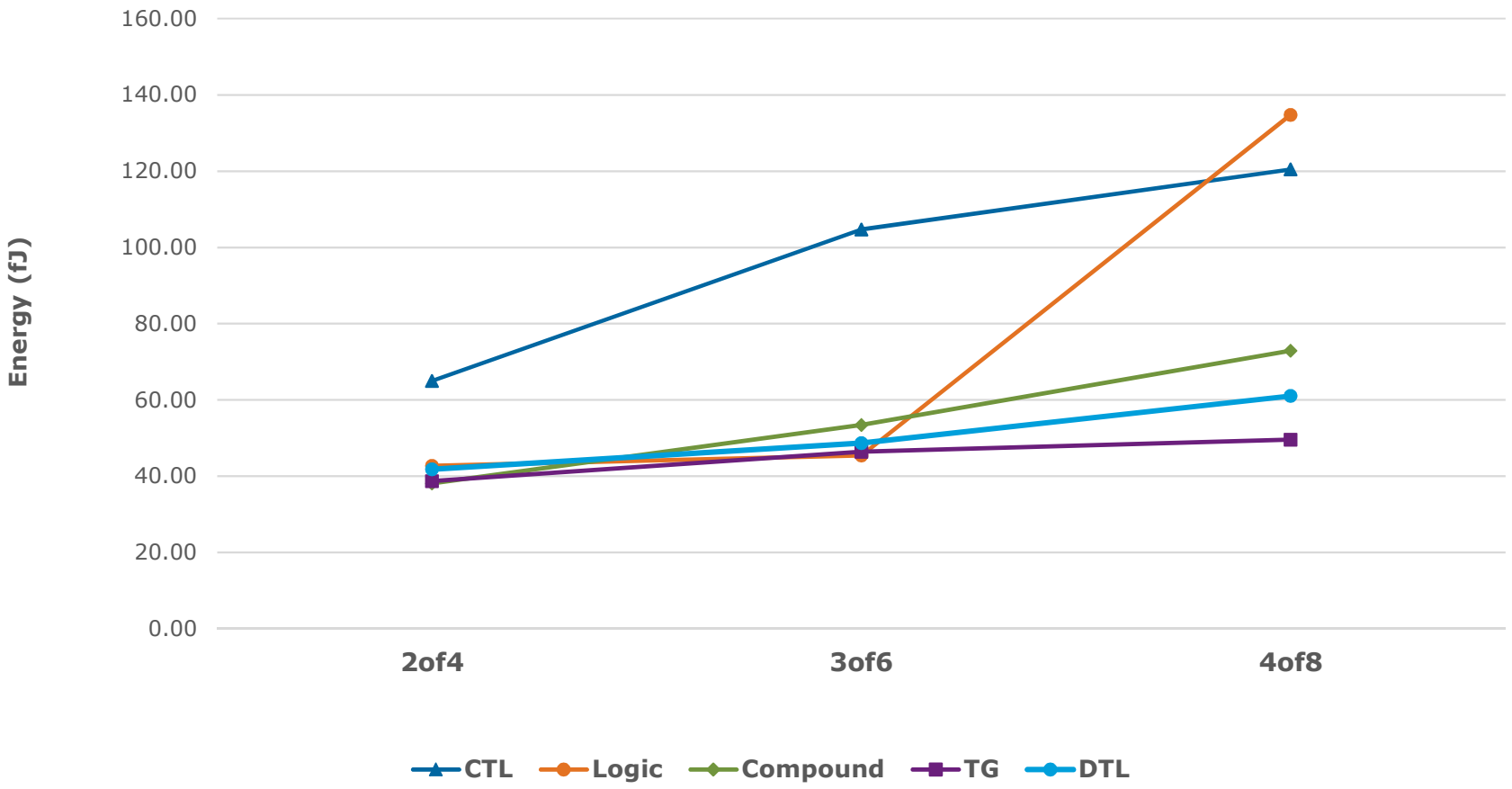
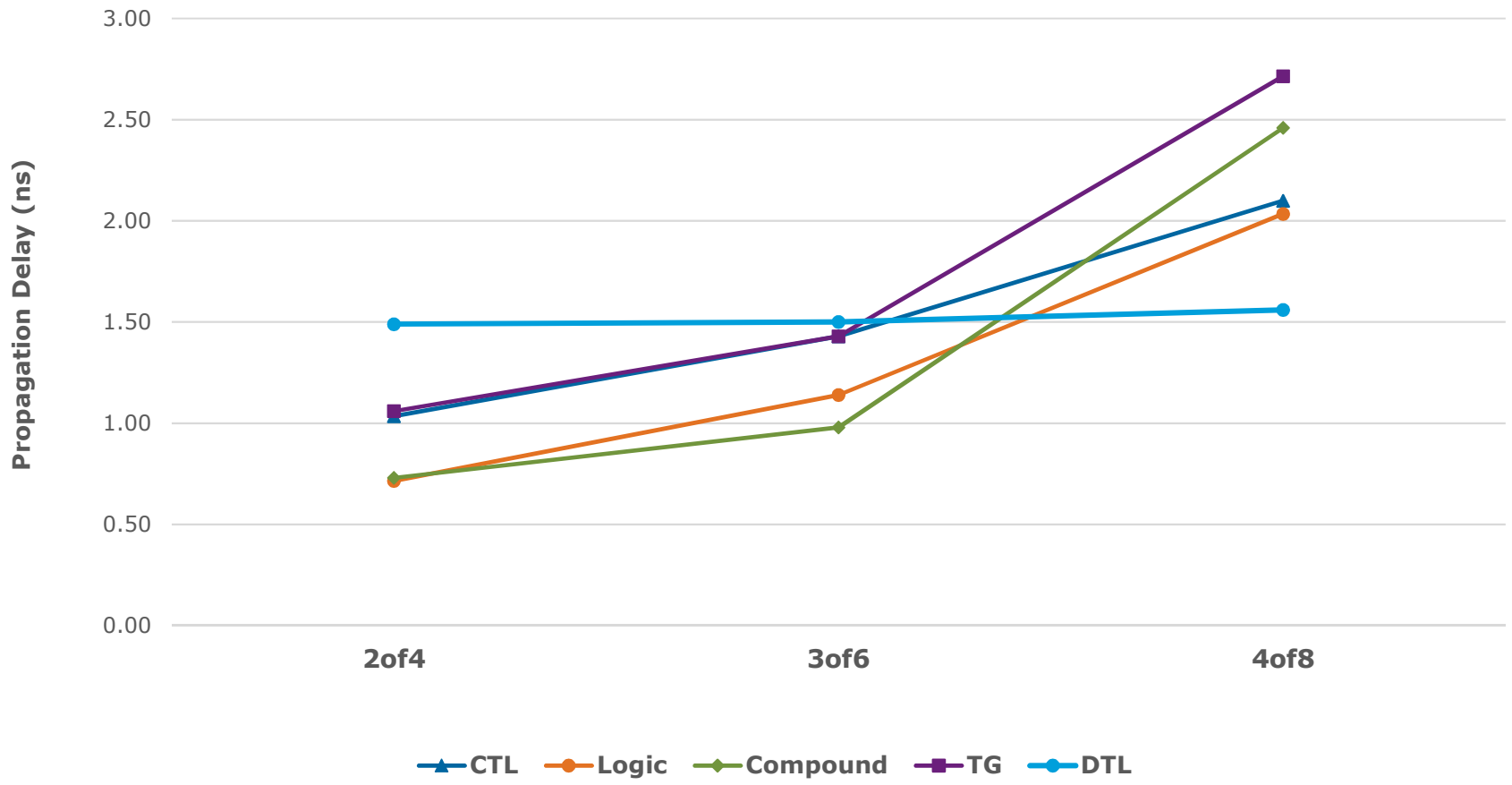
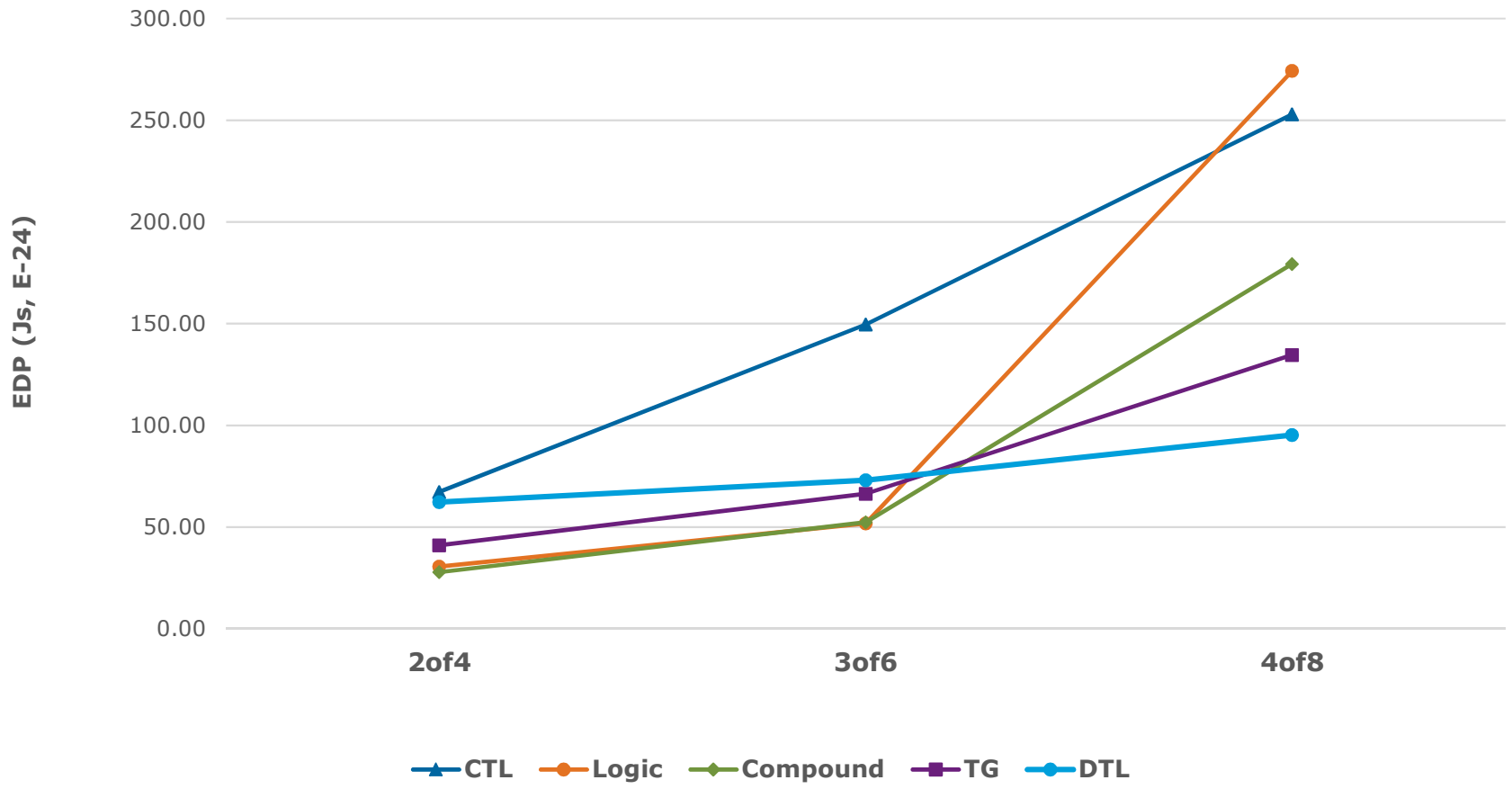
Simulation Results: Energy (Lower is better)



Simulation Results: Delay (Lower is better)



Simulation Results: EDP (Lower is better)



Simulation Observations

- Energy: DTL, XTL and Compound-TL have lowest rate of energy consumption increase with the size of threshold detection
  - CTL consumes more mainly due to shorted inverter
- Delay: DTL has much better delay profile than the rest, followed by Logic Gate-TL and CTL
  - Min period for DTL does not change as it has fewest number of transistors and robustness
- EDP: Due to minimum delay and relatively lower energy consumption, DTL has best EDP so far
  - CTL has large energy consumption as # of inputs (capacitance) increase and requires more time for precharge

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Summary - I

- Since it is a fundamental function and is not yet covered much in literature, threshold detection is the focus of this work
- In fact, our team previously presented ABACUS multiplier architecture which uses parallel carries more than that of a Wallace Tree
  - Performance of ABACUS heavily depends on the performance of large TL detection sub circuits

Summary - II

- Gürdür et. al [2] reported full adder based analysis for different multipliers, indicating
  - ABACUS could compete with Wallace in EDP if the large TL circuits in its core could operate 20% faster
- Need larger input sizes at the core – size 8 or higher (which will exist in an 8x8 multiplier, or larger)
- Our initial results indicate that differential based TL already provides more than 20% advantage in EDP than other approaches

Future Work

- Design, implementation & simulation of Domino-Based TL
  - Where will it stand in the energy-delay analysis
- Investigation of EDP impact of low EDP threshold circuits to multiplier implementations
  - e.g. ABACUS
- Further optimization where necessary
- Increase # of inputs for improved energy-delay trends
- Fabrication & testing of the designs

References

[1] Muhtaroglu, A. (2010). "ABACUS: A novel array multiplier-accumulator architecture for low energy applications," Proceedings of International Conference on Energy Aware Computing (ICEAC), IEEE.

[2] Gürdür, D., "Architectural Assesment of ABACUS Multiplier with Respect to Other Multipliers," M.S. Thesis, Sustainable Environment and Energy Systems Graduate Programme, METU NCC, July 2013.

[3] D. Hampel, K. J. Prost, and N. R. Scheinberg, "Threshold Logic Using Complementary MOS Device," U.S. Patent 3 900 742, Aug. 19, 1975.

[4] J. M. Quintana, M. J. Avedillo, R. Jiménez, and E. Rodríguez-Villegas, "Practical low-cost CPL implementations of threshold logic functions," in *Proc. Great Lakes Symp. VLSI*, West Lafayette, 2001, pp. 139–144.

[5] Y. Leblebici, F. K. Gürkaynak, and D. Mlynek, "A compact 31-input programmable majority gate based on capacitive threshold logic," in *Proc.Int. Symp. Circuits & Systems ISCAS'98*, vol. 2, Monterey, CA, 1998, pp. 105–108.

[6] Y. Leblebici, H. Özdemir, A. Kepkep, and U. Çilingiroglu, "A compact high-speed (31, 5) parallel counter circuit based on capacitive thresholdlogic gates," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1177–1183, Aug. 1996.

[7] Baugh, C. R., Wooley, B. A., "Statistical Analysis of a Differential Threshold Logic Configuration," IEEE Transactions on Computers, Vol. C-25, No.7, 1975 pp. 745-754.

Thank you