Power-Delay Analysis of an ABACUS Parallel Integer Multiplier VLSI Implementation

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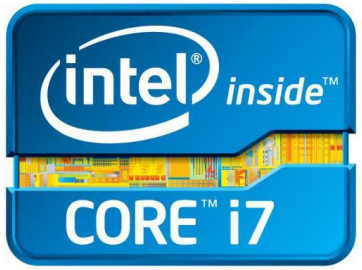
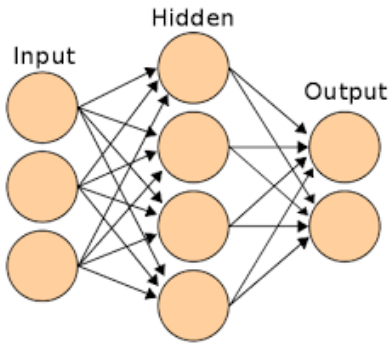
Outline

- Introduction
- Motivation
- WTM vs. ABACUS Compression
- Column Compression Logic
- Theoretical Power/Delay Estimation
- Simulation Results
- Conclusion and Future Work

Introduction

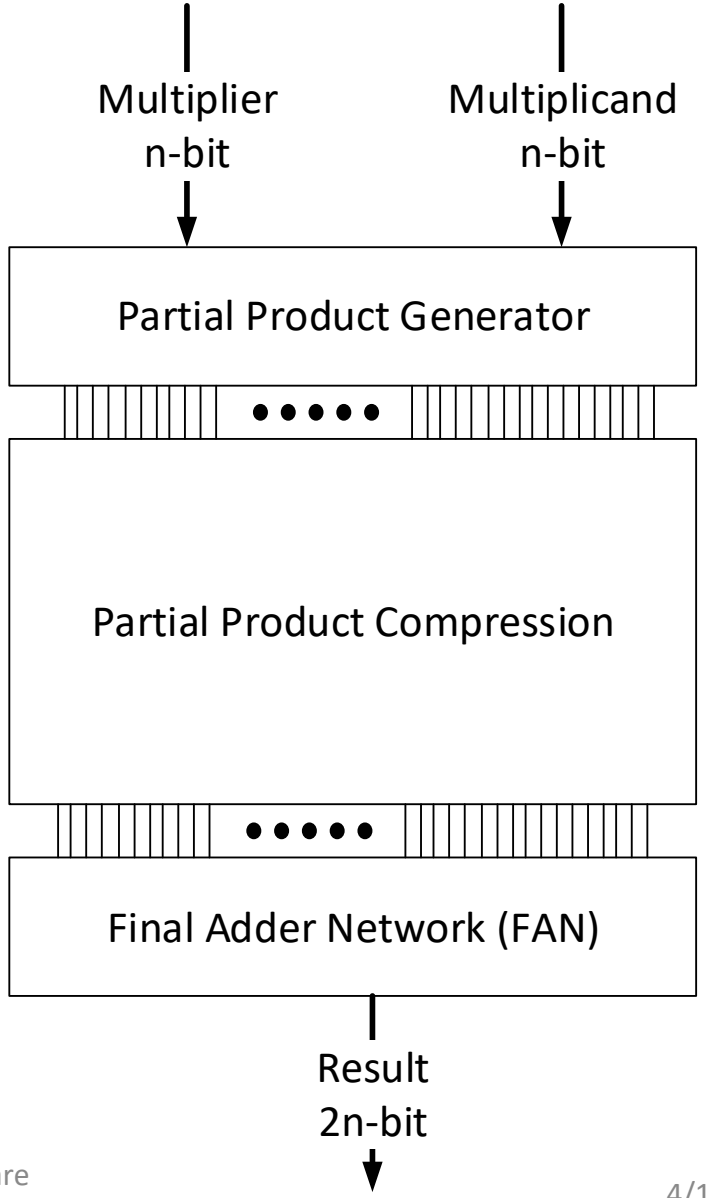
- Significance of power consumption in computing platforms
  - Shrinking platform sizes (i.e. mobile computing)
  - Battery life (i.e. green computing, extended use)
- Binary multiplication as a significant research area
  - Areas of use (i.e. ALU, tracking algorithms, neural networks)
  - A bottleneck on power/performance (large device count)





Parallel Integer Multiplication

- Three stages introduced by Wallace *[1]:
  - Partial Product Generation
  - Partial Product Compression
  - Final Adder Network (FAN)
- Compression stage outputs two rows for FAN
- Compression and FAN have been primary focus on improvement *[1]



*1 C. S. Wallace, "A suggestion for a fast multiplier," IEEE Transactions on Electron. Comput., pp. 114-117, 1964.

Parallel Multiplication in Literature

- Anitha et al. *2 reported ~40% power reduction by combining WTM and Dadda methods (2014)
  - Dadda is used for the outputs of WTM modules.
- Arunachalem et al. *3 proposed a methodology for reducing compression workload, yielding 21% performance improvement (2013)
  - Improvement due to use of Skalansky adders of WTM.
- Rajaram et al. *4 used parallel prefix adders to reduce delay in the FAN (2011)
  - Achieved by reducing compression complexity and fast adders at FAN.

- Chinese Abacus Multiplier *5 is based on an ancient Chinese numeric system, and irrelevant to this study

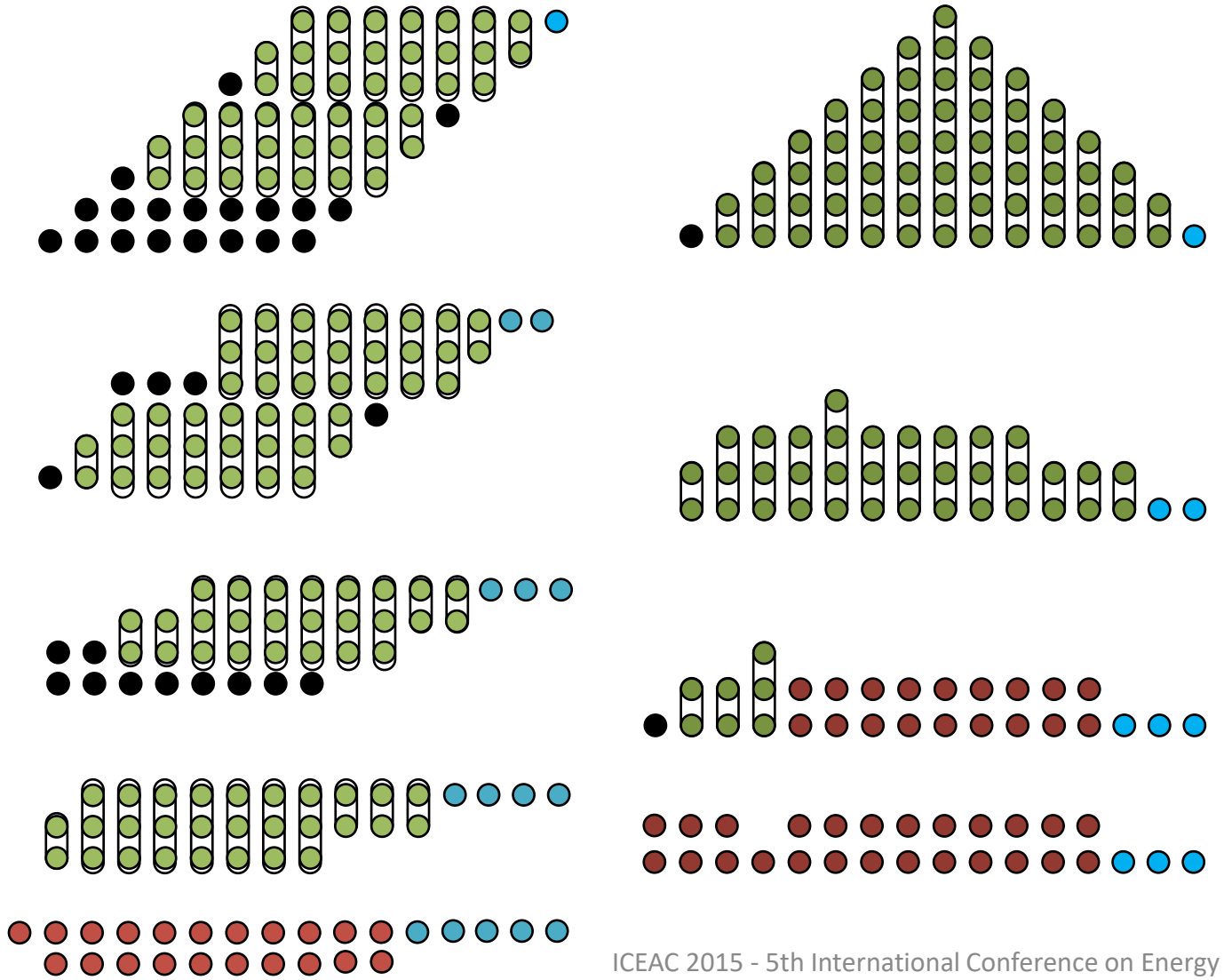
*2 P. Anitha and P. Ramanathan, "A new hybrid multiplier using Dadda and Wallace method," in Electronics and Communication Systems (ICECS), 2014 International Conference on, 2014.

*3 T. Arunachalam and S. Kirubaveni, "Analysis of high speed multipliers," in Communications and Signal Processing (ICCSP), 2013 International Conference on, 2013.

*4 S. Rajaram and K. Vanithamani, "Improvement of Wallace multipliers using parallel prefix adders," in Signal Processing, Communication, Computing and Networking Technologies, 2011 International Conference on, 2011.

*5 Y. Lin, C. Lin, Z. Zhao, Y. Xie, Y. Chen, S. Yi., “A novel high speed Chinese abacus multiplier”, in Proceedings of the International MultiConference of Engineers and Computer Scientists, March 2007.

WTM vs. ABACUS Compression



(8x8)/(16x16)	WTM	ABACUS
#of Stages	4/8	3/3
Ready bits @ final compression	5/6	3/3
Pairs subject to FAN	11/26	13/29

Legend

- Subject to Compression
- Finalized Bit
- Ready for FAN
- Unused Bit

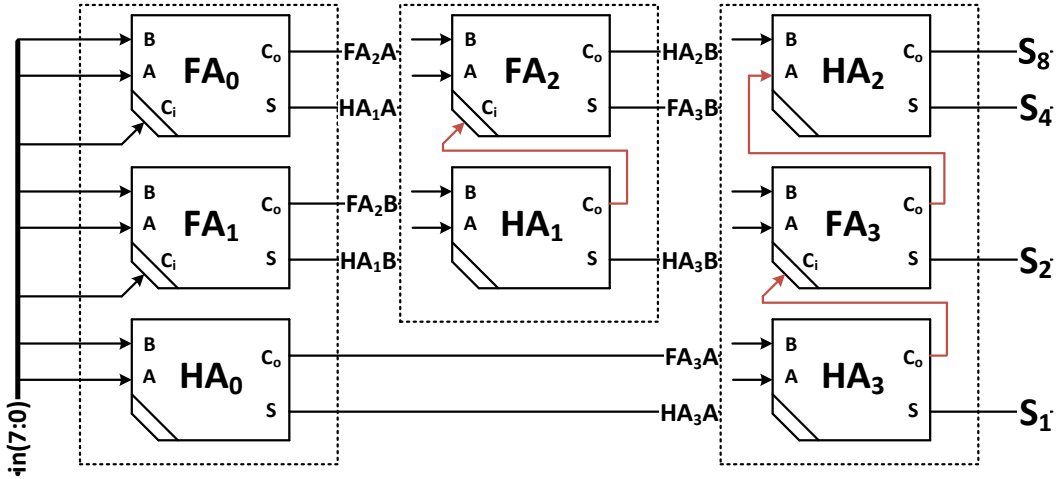
Motivation

- Prior work *[6] addressed ABACUS requires ~20% performance improvement on mid-column compressor to have competitive EDP profiles with WTM
- ABACUS has fewer architectural compression stages than WTM
- Compression architecture enables 'parallel' and 'further carry bits
  - i.e. a 6/n count forwards one rank:+1 and one rank:+2 carries
  - i.e. an 8/n count forwards a rank:+3 carry

*6 D. Gürdür, "Architectural assessment of ABACUS multiplier with respect to other multipliers," M.S. Thesis, Sustainable Environment and Energy Systems Graduate Programme, METU NCC, 2013.

Column Compression Logic

- Full Adder based counters
- Optimized for power/performance
- Figure: 8-bit counter



- Requires more hardware for CCL
- Ripples inside CCL counters

ABACUS vs. WTM (Architectural)

+ Fewer number of architectural stages
+ Parallel and further carries from CCL cells

- More number of devices *(due to internal CCL-architecture)*
- Carry ripples inside CCLs *(due to internal CCL-architecture)*

Theoretical Power/Delay Estimation Methods

- Linear Delay Model (LDM)
  - $D = N \times F^{1/N} + P$
    - N: number of gates on critical path
    - F: path effort
    - P: parasitic delay (RC of fanout)
- Static power is estimated with 'scaled' # of devices
  - $P_{stat} = I_{stat} \times V_{DD}$; I_{stat} ~ W/L of MOSFETs
- Activity factor is extracted from dynamic power estimation
  - $P_{dyn} = C_{tot} \times V_{DD}^2 \times f \times \alpha$

Theoretically Estimated Results

- Performance: ABACUS and WTM have competitive profiles
  - D_{ABACUS} = **84.25** D_{WTM} = **90.36** (with $FFxFF_{hex}$ input vector case)
- Static power: WTM is superior than ABACUS
  - $P_{stat,WTM}/P_{stat,ABACUS}$ = **119%**
- Dynamic power: Extracted minimum activity factor requirement
  - Required $\alpha_{ABACUS}/\alpha_{WTM}$ is **84%**
- Area: WTM is more area efficient than ABACUS
  - WTM is **1/5** more area efficient than ABACUS

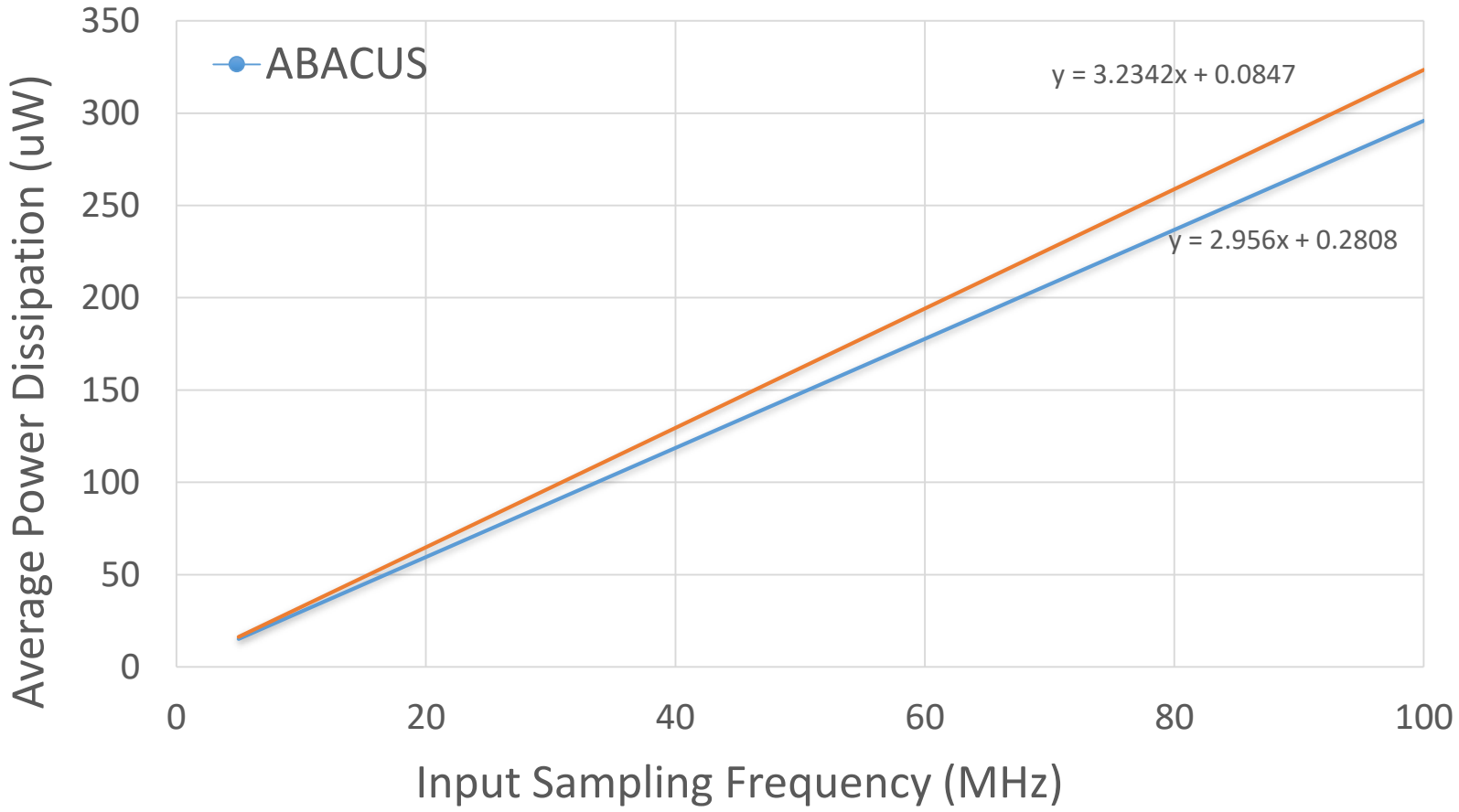
Test Vectors for Simulation

Vector Name	Multiplicand	Multiplier
Full	1111 1111	1111 1111
Empty	0000 0000	0000 0000
Checkboard1	0101 0101	0101 0101
Checkboard2	0101 0101	1010 1010
Checkboard3	1010 1010	0101 0101
Checkboard4	1010 1010	1010 1010
Pattern1	0011 0011	0011 0011
Pattern2	1100 1100	0011 0011
Pattern3	1100 1100	1100 1100
Random1	0111 0100	1001 1110
Random2	1011 1101	0011 1011
Random3	0101 1101	0111 0010

Simulation Details

- UMC 180nm technology
- V_{DD} = 1.2 V
- Aspect ratio: 2.5/1
- Various operating frequencies (5, 10, 25, 50, 100 MHz)

Results: Average Overall Power Dissipation



$y = ax + b$

$P_{tot} \sim C_{dyn} * f + P_{stat}$

$P_{stat,WTM} = 0.084\ \mu W$

$P_{stat,ABACUS} = 0.281\ \mu W$

$C_{dyn,WTM} \sim 3.234$

$C_{dyn,ABACUS} \sim 2.956$

Results: Power/Delay Measurements

(8x8)	ABACUS	WTM	improvement%
Delay (ns)	3.37	3.37	---
P_{static} (nW)	280.8	84.7	-231.5%
PDP (100 MHz, fJ)	997	1090	8.6%
Device Count	4374	3456	-26.6%
C_{dyn} (uF)	2.463	2.695	8.6%
Activity Factor	5.631	7.799	27.8%

(8x8)	WTM	ABACUS
#of Stages	4	3
Ready bits @ final compression	5	3
Pairs subject to FAN	11	13

(16x16)	WTM	ABACUS
#of Stages	8	3
Ready bits @ final compression	6	3
Pairs subject to FAN	26	29

Conclusion

- ABACUS is analyzed, implemented and compared against WTM in terms of power/performance
- Performance gap of ABACUS is filled (w.r.t. WTM, [7])

- WTM has lower static power dissipation and device count
- ABACUS proves lower overall average power due to less activity
- Worst-case propagation delay is same for both architectures

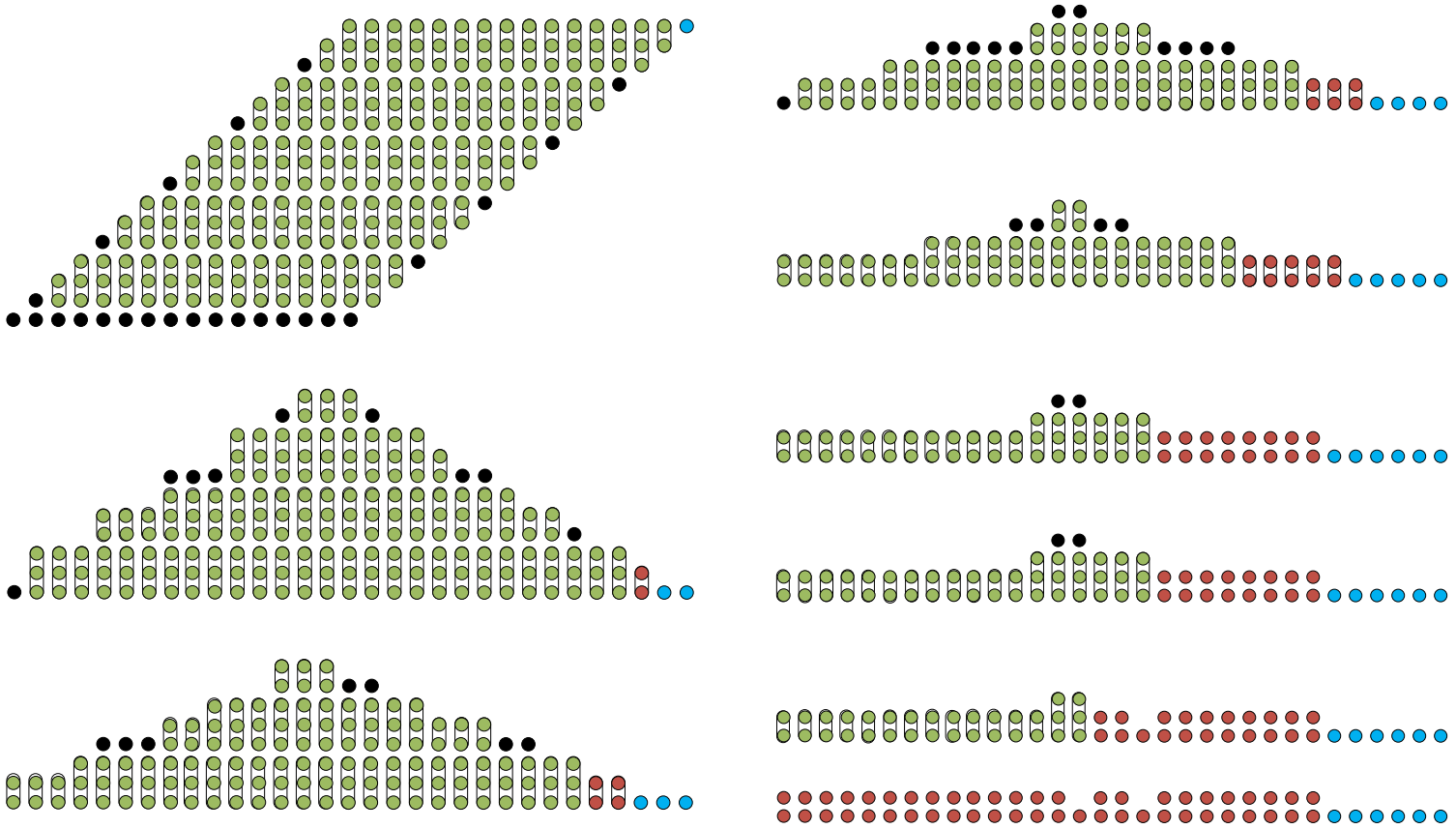
Future Work

- Larger operands are needed to extract accurate trend lines
  - i.e. 16x16, 32x32 bit multiplication
- With larger operand sizes;
  - ABACUS is expected to have lower power dissipation
    - (due to activity factor)
  - ABACUS is expected to have lower propagation delay
    - (due to lower number of stages)
- Proposed CCL (e.g. counter) is subject to optimization
  - i.e. less ripples (delay/activity factor)
  - i.e. less devices (power/performance)

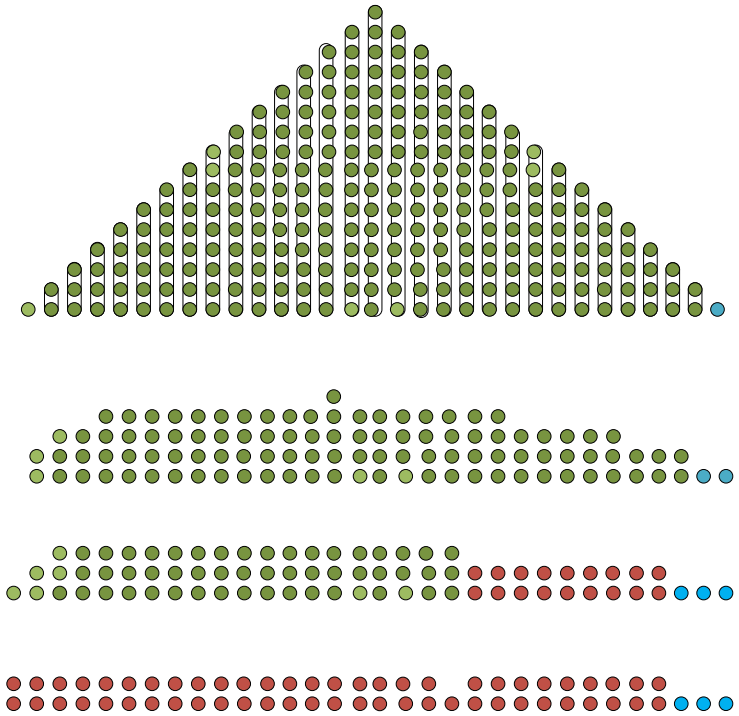
Thank you

Backup/Extras

16x16 WTM



16x16 ABACUS



Simulated Delay Results (ns)

	Delay (ns)		
Test Vector Name	ABACUS	WTM	%
Full	3.25	2.64	23.11%
Empty	2.38	1.76	35.23%
Checkboard1	2.75	2.8	-1.79%
Checkboard2	2.98	3.37	-11.57%
Checkboard3	3.01	2.81	7.12%
Checkboard4	3.37	3.36	0.30%
Pattern 1	2.92	3.02	-3.31%
Pattern 2	2.67	2.83	-5.65%
Pattern 3	2.68	3.17	-15.46%
Random 1	3.29	3.01	9.30%
Random 2	3.08	2.92	5.48%
Random 3	2.71	2.82	-3.90%

Simulated Power Results

Average I	Frequency (MHz)				
(uA)	100	50	25	10	5
ABACUS	246.5	123.5	61.91	24.84	12.45
WTM	269.6	134.8	67.47	27.03	13.54

Average P	Frequency (MHz)				
(uW)	100	50	25	10	5
ABACUS	295.8	148.2	74.292	29.808	14.94
WTM	323.52	161.76	80.964	32.436	16.248

PDP	Frequency (MHz)				
(fJ)	100	50	25	10	5
ABACUS	996.84	499.43	250.36	100.45	50.34
WTM	1090.26	545.13	272.84	109.30	54.75

Current Study: Real Time Tests of 8x8 ABACUS/WTM with UMC 180nm technology