Comparative Power-Delay Performance Analysis of Threshold Logic Technologies

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Outline

- Introduction
- History
- Areas of Use
- Motivation
- Threshold Logic (TL) Technologies
- Evaluation (Testing) Methods
- Simulation Results
- Summary

Introduction

- Threshold Logic (TL) detects if number of inputs exceed a pre-defined threshold number

$$m(\Theta) = 1 \text{ if } \sum_{i=0}^{n} x_i \geq \Theta$$

  - Θ: Threshold number
  - n: Number of inputs
  - m: threshold function
  - x_i: input
- Although they were first introduced in 1960s, gained popularity in 2000s
- Considered to be an alternative to Boolean Logic (BL)
  - e.g. possesses 'greater logic power' *1

*1 D. Hampel and R. O. Winder, "Threshold logic," *Spectrum, IEEE,* vol. 8, no. 5, pp. 32-39, 1971.

History of TL

- TL technologies didn’t gain popularity until 2000s
  - Hampel asked ‘why not use TL instead of BL?’
- Beiu et al.*[2] answered Hampel’s question (2003) in their survey
  - Lack of TL synthesis tools
  - Less robust for manufacturing, more customization (i.e. time)
- (2004) Design automation tools *[3]
- (2007) Synthesis & verification tools *[4]
- (2008) Test pattern generation algorithms *[5]

} Developments for TL upon Beiu’s survey

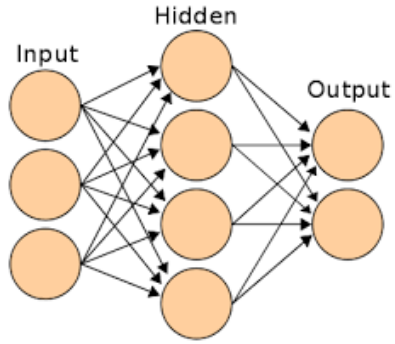
*[1] V. Beiu, J. Quintana and M. Avedillo, "VLSI implementations of threshold logic-a comprehensive survey," *Neural Networks, IEEE Transactions on*, vol. 14, no. 5, pp. 1217-1243, 2003.

*[2] R. Zhang, P. Gupta, L. Zhong and N. Jha, "Synthesis and optimization of threshold logic networks with application to nanotechnologies," *Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings*, vol. 2, pp. 904-909, 2004.

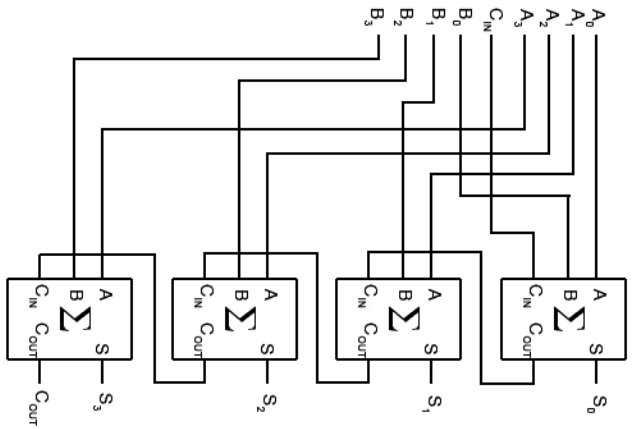
*[3] T. Gowda, S. Vrudhula and G. Konjevod, "Combinational equivalence checking for threshold logic circuits," *Proceedings of the 17th ACM Great Lakes symposium on VLSI*, pp. 102-107, 2007.

*[4] P. Gupta, R. Zhang and N. Jha, "Automatic Test Generation for Combinational Threshold Logic Networks," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 16, no. 8, pp. 1035-1045, 2008.

Areas of Use



- Artificial Neural Networks (ANN)
  - Use of software/FPGA are not energy efficient
- Arithmetic Applications
  - i.e. addition, multiplication, threshold
- Binarization
  - Evaluation of pixels (or matrices) with pass/fail threshold



- Use of TL is still rare
- BL/software is preferred

Threshold Logic in Literature

- Implementation with complementary pass transistors *[6]
  - Quintana et al.: Advantageous on low power
- TLs based on capacitive networks *[7-9]
  - Leblebici et al.: Advantageous on delay/area over Boolean Logic
- Differential/Mirror based TL implementations *[10-11]
  - Avedillo et al.: Trade-offs over delay, area, power
- Other technologies:
  - Single-electron technology (SET)
  - Resonant-tunneling diode (RTD)
  - Memristor-based implementations

*6 J. M. Quintana, M. J. Avedillo, R. Jimenez and E. Rodrigues-Villegas, "Practical low cost implementations of threshold logic functions," *GLSVLSI, ACM,* 2001.
*7 H. Ozdemir, A. Kepkep, B. Pamir, Y. Leblebici and U. Cilingiroglu, "A capacitive threshold-logic gate," *IEEE Journal of Solid-State Circuits,* vol. 31, no. 8, pp. 1141-1150, 1996.
*8 A. Schmid and Y. Leblebici, "Realisation of multiple-valued functions using the capacitive threshold logic gate,," *Computers and Digital Techniques, IEE Proceedings,* vol. 151, no. 6, pp. 435-447, 2004.
*9 J. López-García, J. Fernández-Ramos and A. Gago-Bohórquez, "A balanced capacitive threshold-logic gate," *Analog Integrated Circuits and Signal Processing,* vol. 40, no. 1, pp. 61-69, 2004.
*10 M. Padure, S. Cotofana, S. Vassiliadis, C. Dan and M. Bodea, "A low-power threshold logic family," in *9th International Conference on Electronics, Circuits and Systems.*, 2002.
*11 M. J. Avedillo, J. Quintana, A. Rueda and E. Jimenez, "Low-power CMOS threshold-logic gate," *Electronics Letters,* vol. 31, no. 25, pp. 2157-2159, 1995.

Motivation

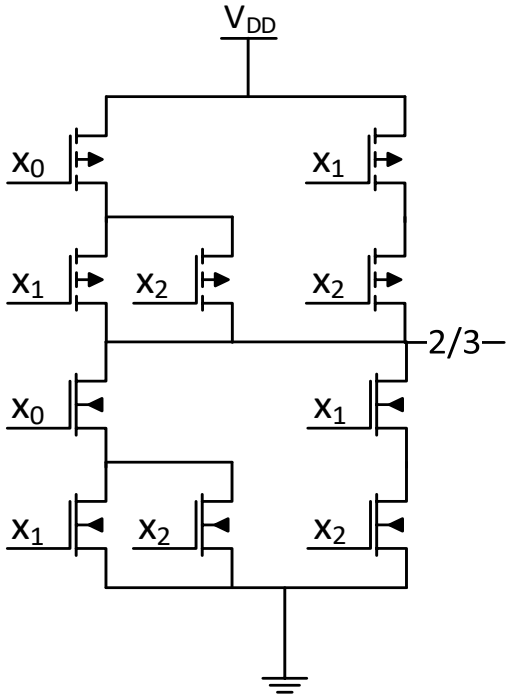
- All TL technologies in literature emphasize criteria based on either
  - Numeric values
  - Comparative values w.r.t. similar implementations or Boolean Logic
- Little work on power/delay comparison of TLs from different circuit families
- A methodology for such comparison is missing
  - It is difficult to gather different technologies for comparison
  - Different technologies require various conditions
    - i.e. clock(s), analog/digital, custom source(s), number/type of outputs
- A fair comparison scenario of comparing various TLs provides valuable insight

Scope of This Study

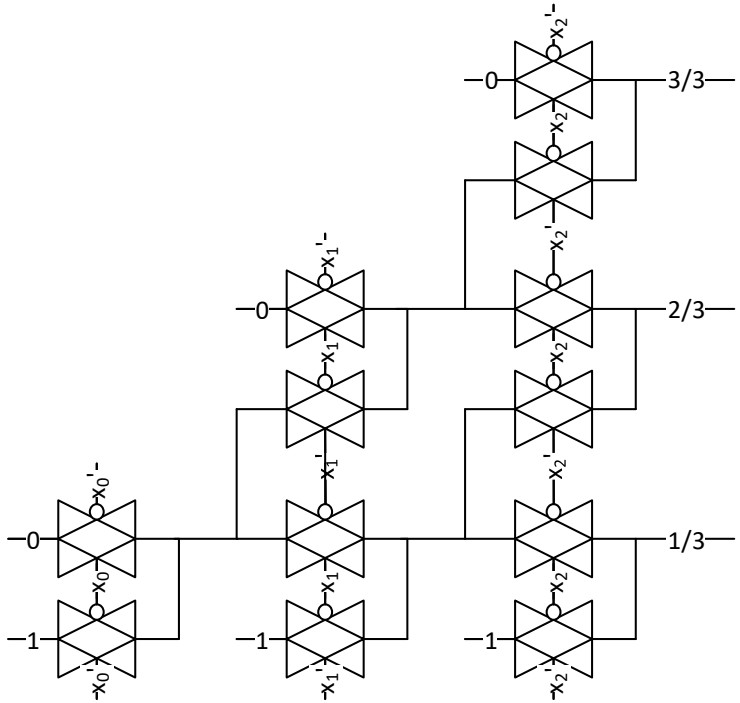
- Capacitive Threshold Logic (CTL) comparison with CMOS-based TL was presented earlier in ICEAC ’13 *[12]
- This work expands the earlier investigation further
- Seven TL technologies are compared on power/performance/area
  - Compound-CMOS (CMOSTL)
  - Boolean (NAND-based) (GTL)
  - Complementary Pass Transistor (CPLTL)
  - Capacitive (CTL)
  - Differential (DTL)
  - Current-Comparator (ITL)
  - Full Adder (FATL)
- A testing scenario is developed for TLs that have specific requirements

*12 F. Ercan and A. Muhtaroglu, "Energy-delay performance of capacitive threshold logic (CTL) circuits for threshold detection," in *Energy Aware Computing Systems and Applications (ICEAC), 4th Annual International Conference on*, 2013.

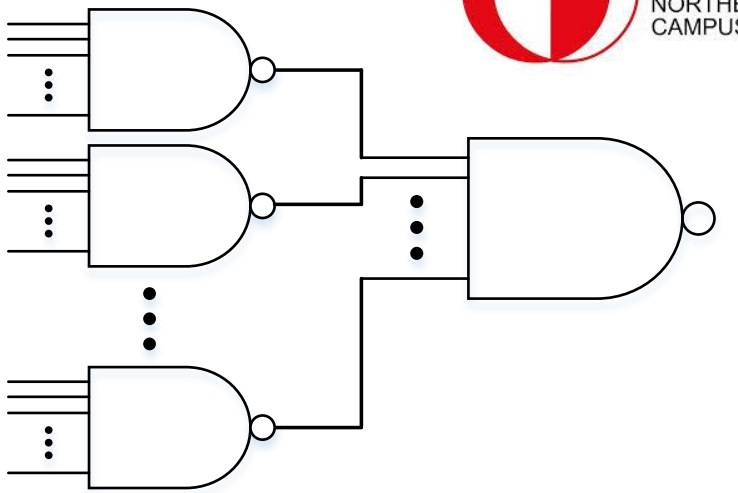
Digital-Based TL Technologies



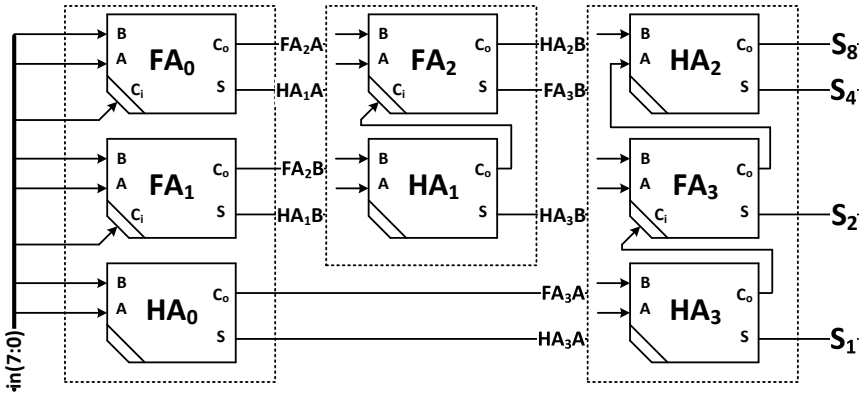
Majority Voter
(CMOSTL)



Complementary Pass
Transistor Based TL
(CPLTL)



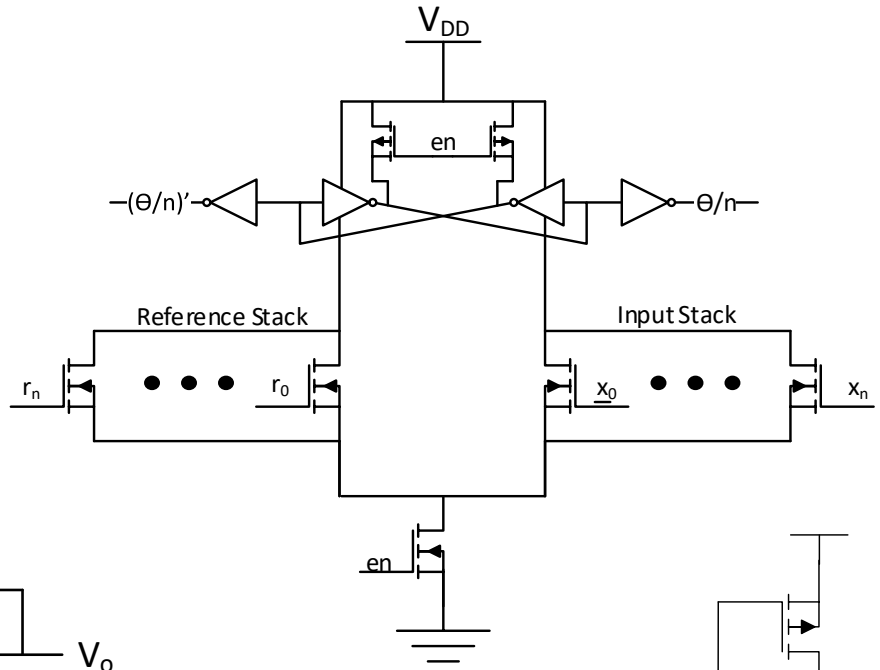
Boolean Gate Based TL
(GTL)

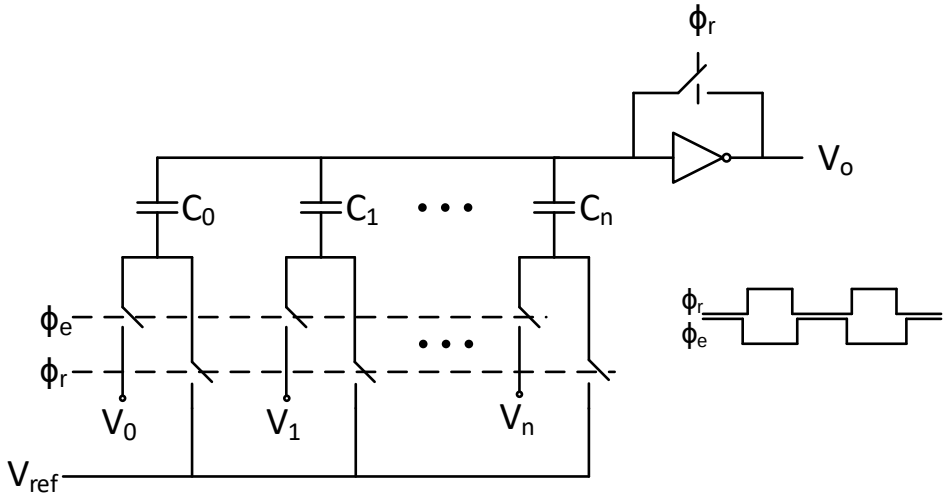


Adder Based Parallel Counter
(FATL)

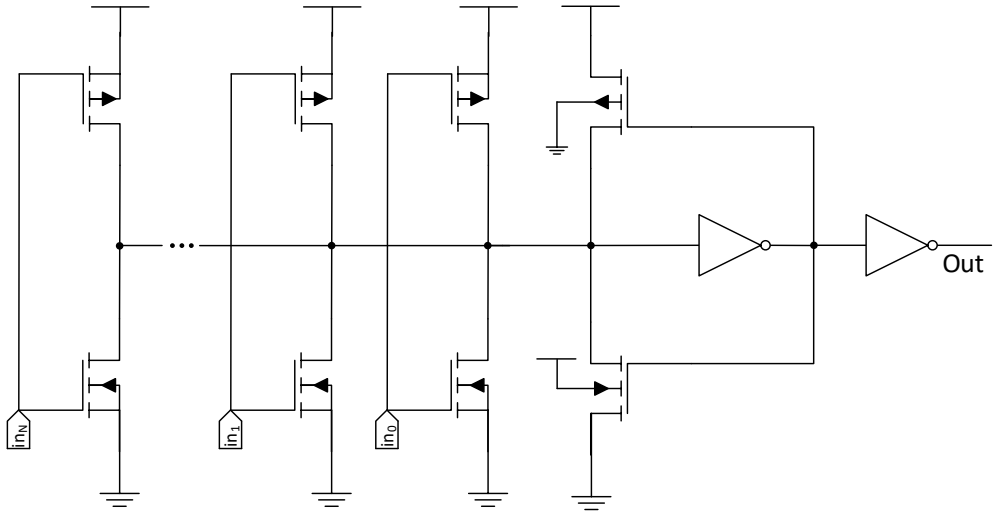
Analog-Based TL Technologies

Differential Threshold Logic (DTL)





Capacitive Threshold Logic (CTL)

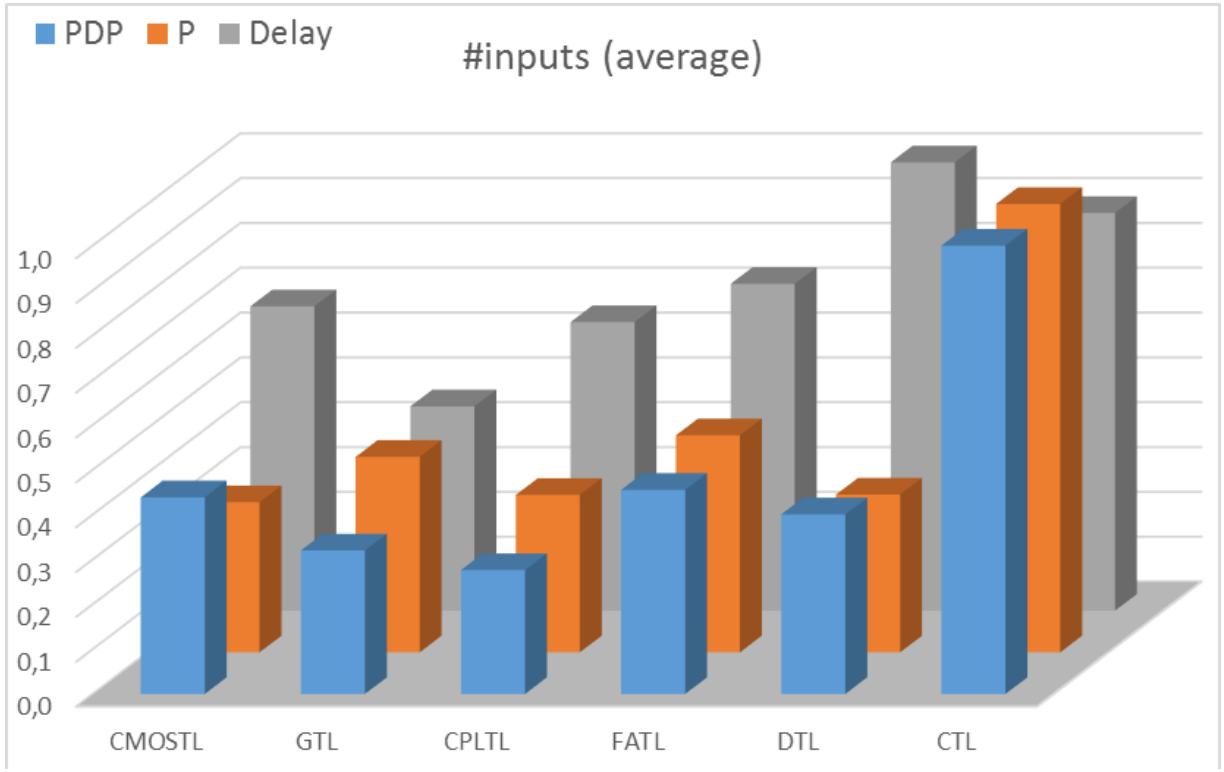


Current-Based Threshold Logic (ITL)

Evaluation Methods & Requirements

- CTL & DTL require clock signals
  - Need refresh before each evaluation: $t_p = t_{p,rst} + t_{p,eval}$
- Average power dissipation is calculated for various frequencies
  - Extraction of static and dynamic power: $P_{tot,av} = V_{DD}\, I_{stat} + C_{dyn}\, V_{DD}^2\, f$
  - PDP = $P_{tot,av} \times t_p$
- DTL, CPLTL, FATL have multiple outputs
  - Worst-case output is taken into account
- UMC 180nm technology – 2.5/1 Aspect Ratio – Fan-in limit: 4
- Results are categorized w.r.t.:
  - Number of inputs
  - Threshold number

Results: with input number

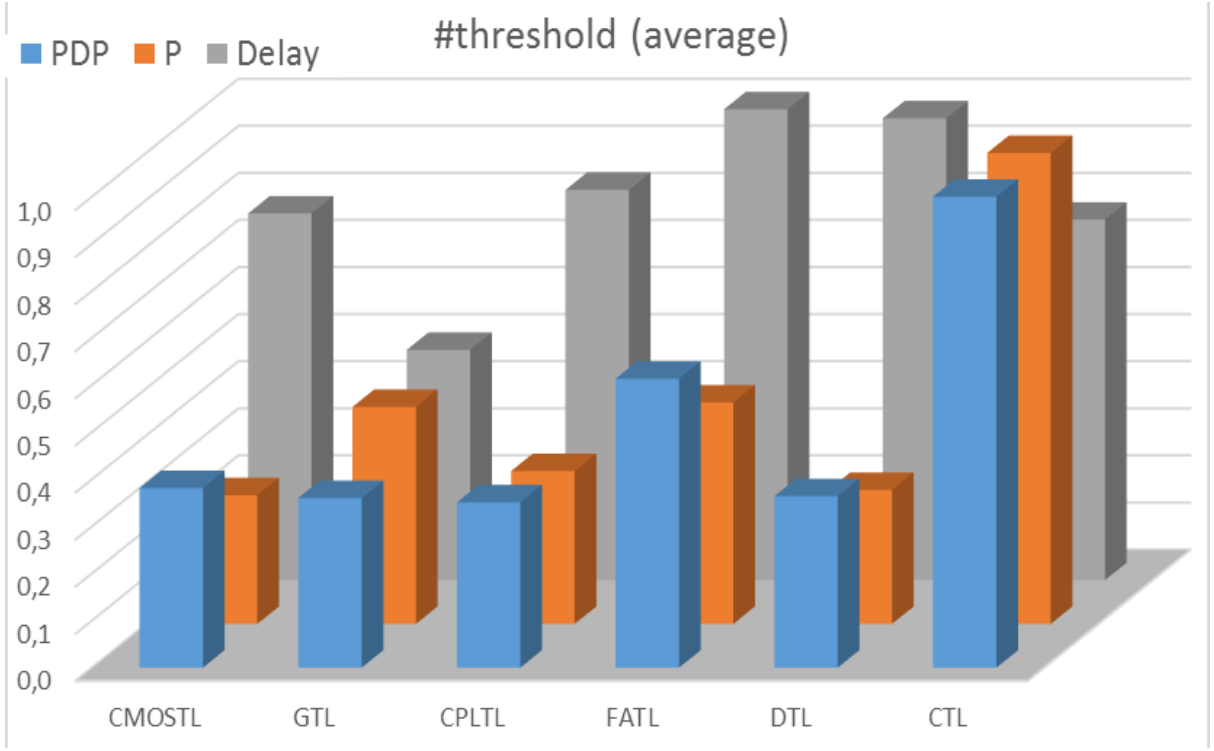


- GTL has 29.2% lower delay than next best case (CPLTL)
- CMOSTL has 4.7% lower P_{av} than next best case (CPLTL)
- CPLTL has 13.6% lower PDP than next best case (GTL)

- DTL has the worst delay profile
- CTL has the worst power/PDP profile followed by FATL (2x)

- **Values are arithmetic averages of varying number of inputs!**
- 1/2, 2/4, 3/6, 4/8 (threshold/input) cases

Results: with threshold number

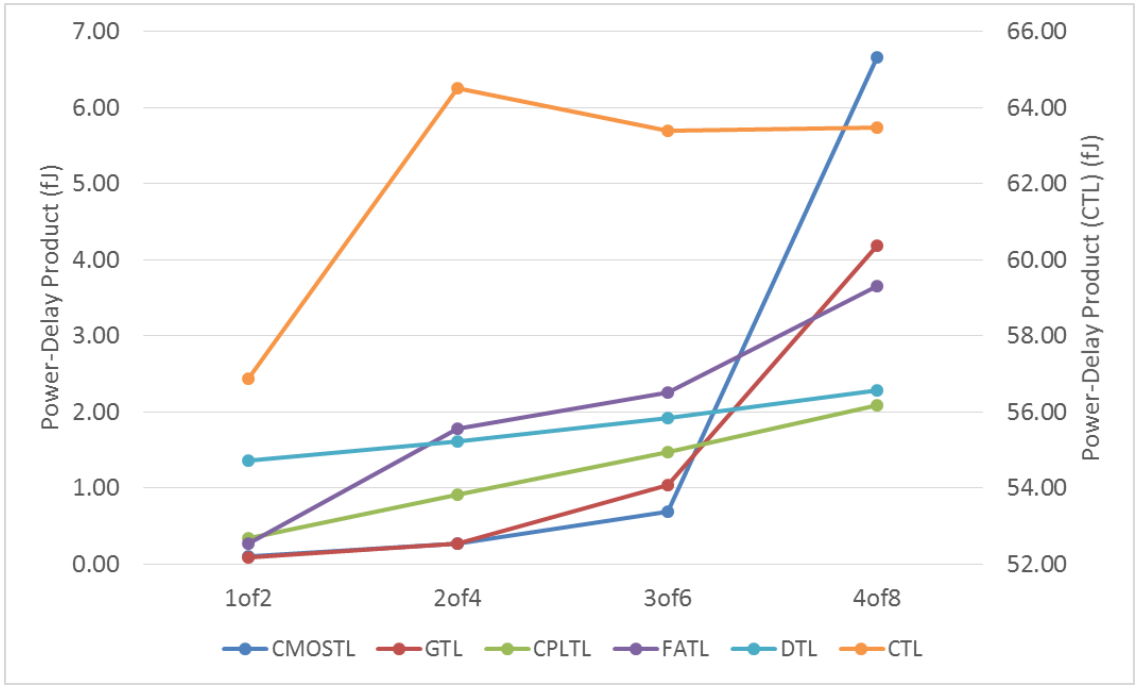


- GTL has 36.1% lower delay than next best case (CTL)
- CMOSTL has 3.8% lower P_{av} than next best case (DTL)
- CPLTL has 2.6% lower PDP than next best case (GTL)

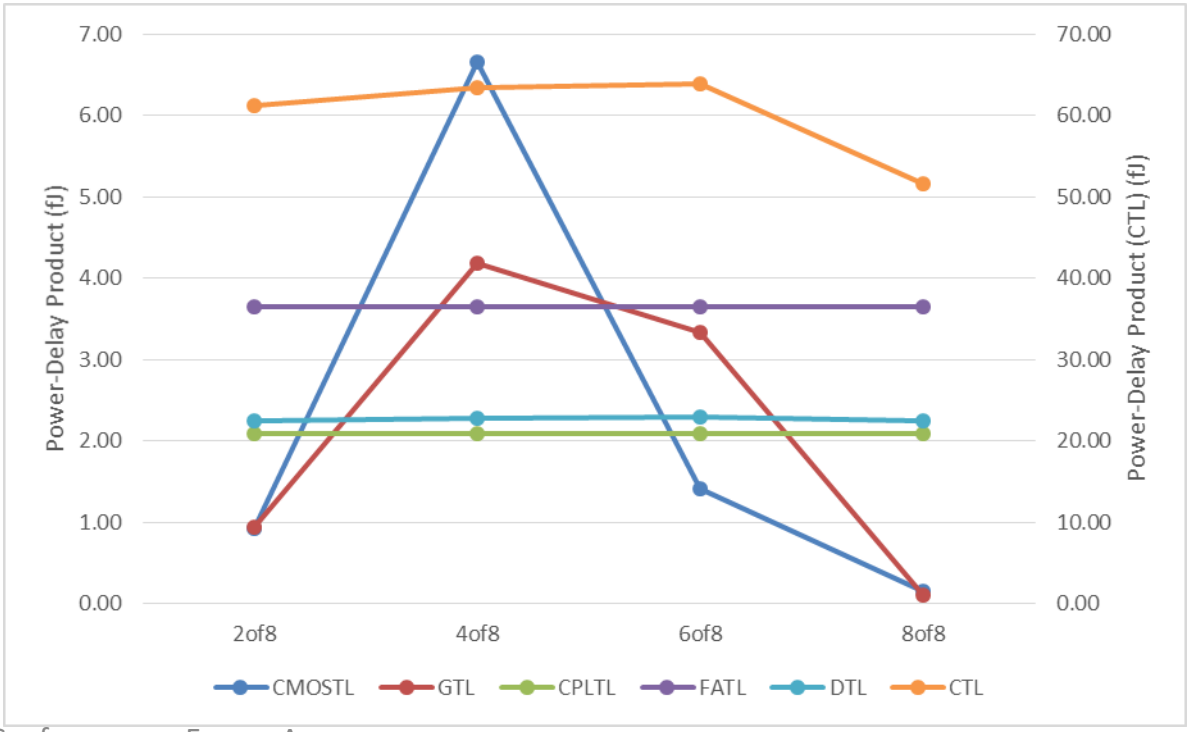
- FATL has the worst delay profile
- CTL has the worst power/PDP profile followed by FATL (2x)

- **Values are arithmetic averages of varying number of threshold!**
- 2/8, 4/8, 6/8, 8/8 (threshold/input) cases

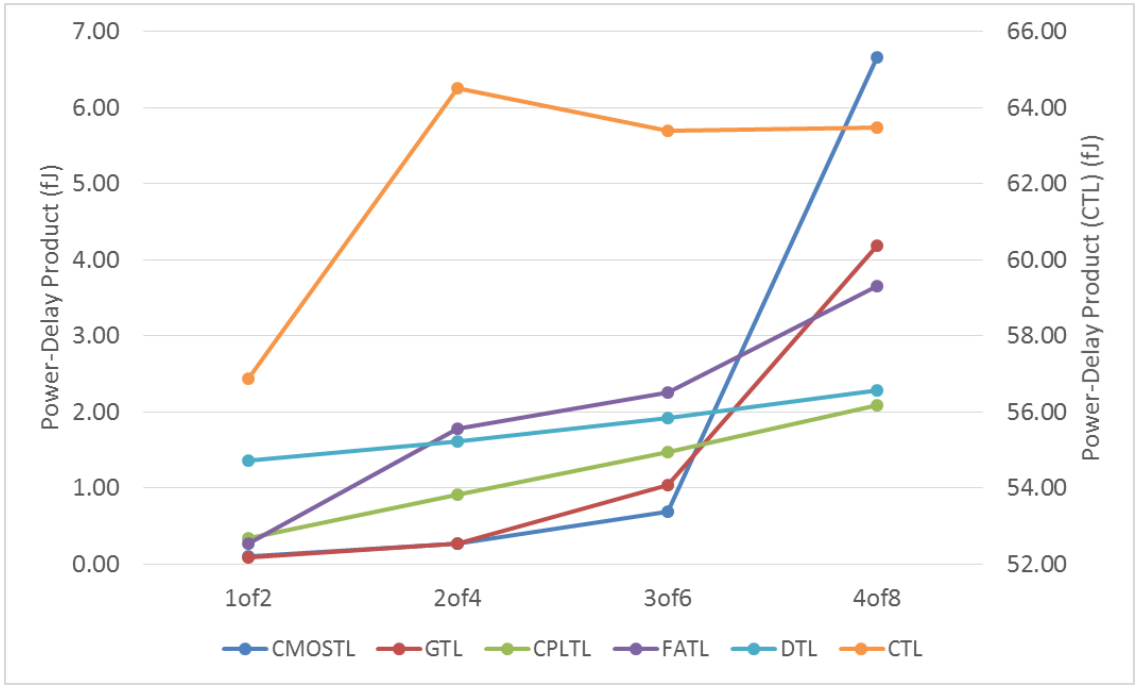
PDP w.r.t. input and threshold numbers

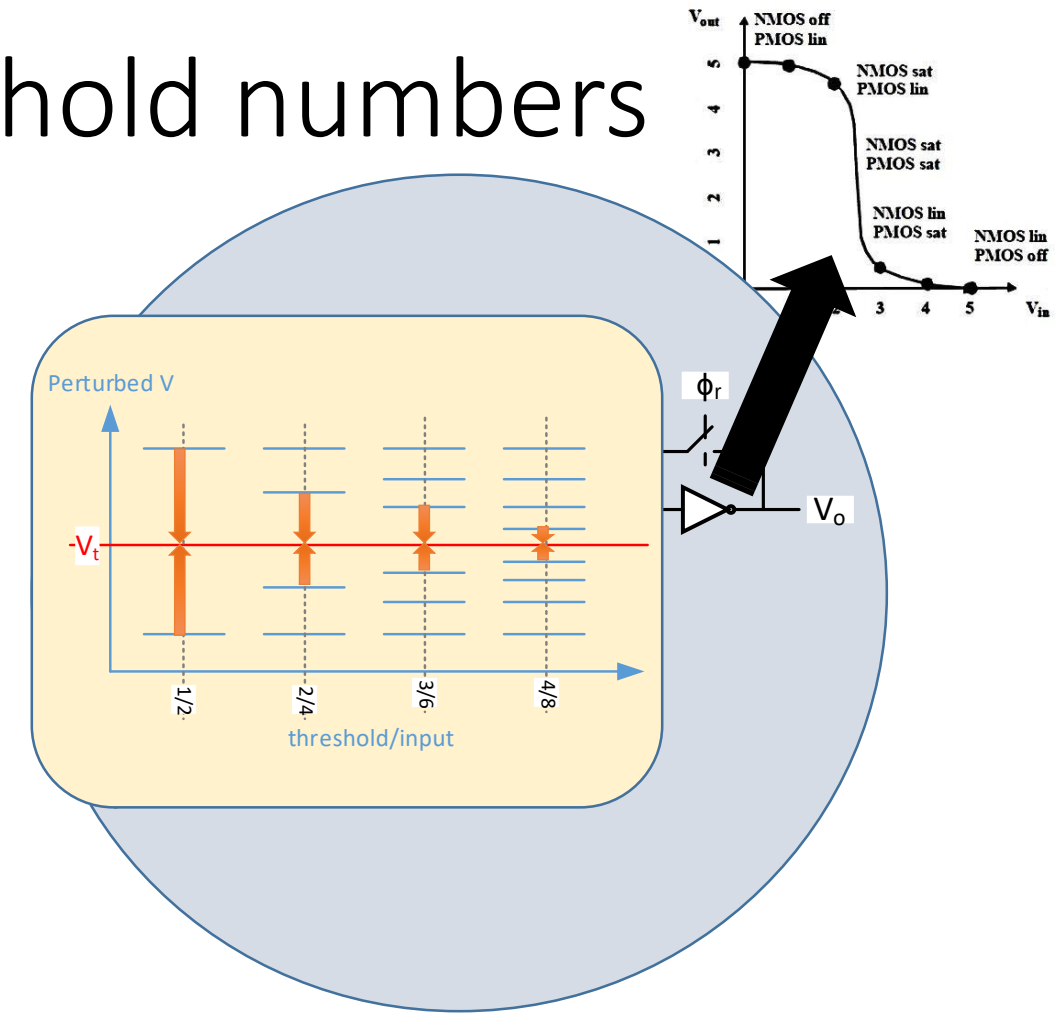


- Large variations (if any) w.r.t. input number / threshold should be taken into account



PDP w.r.t. input and threshold numbers





*Practical variations on perturbed voltage of CTL yields uneven fluctuations in PDP

PDP w.r.t. input and threshold numbers

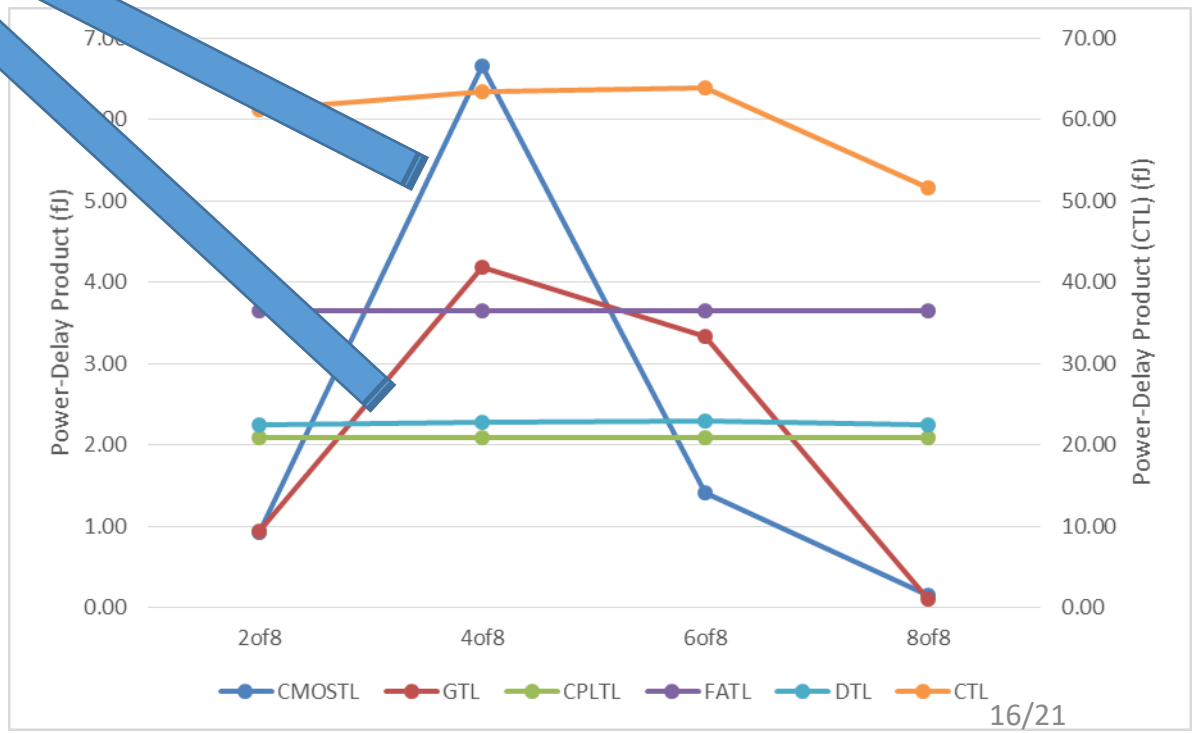
For CMOSTL and GTL:

$\#gates_{input} = comb(n, \Theta)$

Area, power,
delay is the most
when $\Theta = n/2$

Number of MOSFET devices		
	CMOSTL	GTL
2/8	149	364
4/8	**638**	**1900**
6/8	314	1092
8/8	58	46

- Large variations (if any) w.r.t. input number / threshold should be taken into account



Summary Table - Quantitative

AVERAGE STATISTICS, CHARACTERISTICS, APPLICATIONS OF USE OF THRESHOLD LOGIC GATES							
		CMOSTL	GTL	CPLTL	FATL	DTL	CTL
Average Values w.r.t # of inputs	Delay (ns)	0.661	0.444	0.627	0.710	0.974	0.864
	P(µW)	84.03	109.53	88.20	121.59	88.38	251.19
	PDP (fJ)	95.02	69.37	59.89	98.66	86.77	216.69
	# of devices	216	582	124	192	21	50
Average Values w.r.t threshold #	Delay (ns)	0.887	0.557	0.944	1.139	1.117	0.872
	P(µW)	92.57	155.98	109.89	159.17	96.29	338.58
	PDP (fJ)	112.71	106.46	103.74	181.30	107.55	295.57
	# of devices	290	850	234	384	27	77

Summary Table - Qualitative

AVERAGE STATISTICS, CHARACTERISTICS, APPLICATIONS OF USE OF THRESHOLD LOGIC GATES							
		CMOSTL	GTL	CPLTL	FATL	DTL	CTL
Analog/Digital		Digital	Digital	Digital	Digital	Analog	Analog
Need of Reference Voltage		No	No	No	No	No	Yes
Symmetry		N/A	N/A	N/A	N/A	Yes	Yes
Number of Clock Signals		-	-	-	-	1	2
Number of Outputs		1	1	N	$\log_2(N)+1$	2	1
Fan-in		small	small	large	large	large	inter
Applications of TLG use that require	Low power	x	x	✓	x	✓	x
	High performance	x	✓	✓	x	x	x
	Low PDP	x	x	✓	x	✓	x
	Smaller area	x	x	x	x	✓	✓
	Combinational	✓	✓	✓	✓	x	x
	Pipeline	x	x	x	x	✓	✓
	Multi-threshold	x	x	✓	✓	✓	x
	Single-threshold	✓	✓	x	x	✓	x
	Low standby power	✓	✓	✓	✓	x	x

Conclusion

- A comparison scenario is developed to compare TLs from different technologies
- Seven TL technologies are compared against each other on power and performance
- Compared to their next best case;
  - GTL holds 29.2% better delay
  - CMOSTL proves 3.8% lower average power consumption
  - CPLTL provides 2.6% lower PDP

Summary

- GTL is preferable for performance oriented platforms (i.e. servers)
- DTL/CMOSTL are better fit for power oriented platforms (i.e. mobile)
- FATL/CPLTL provides lower power consumption for apps that require multiple threshold outputs
- CPLTL/DTL are more preferable for PDP-oriented platforms (i.e. desktop/notebook)

- This work can be extended to cover more TL implementations from TL technologies
- A more sophisticated testing requirement may be necessary for other TL technologies
- Despite the TL reviews/implementations in literature, without such a cross-comparison scenario that looks into all relevant metrics may be misleading

Thank you