High-Throughput does not Compromise Energy Efficiency:

New Algorithms and Implementations for 5G Polar Codes

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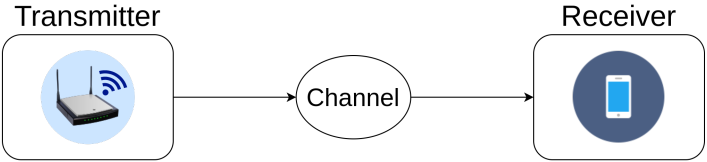
Vice Chair - IEEE Montréal Section
Montréal, QC, Canada

May 6, 2021

Communications & Channel Capacity



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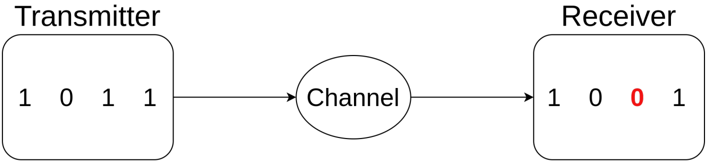

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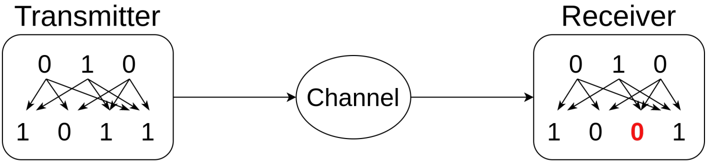

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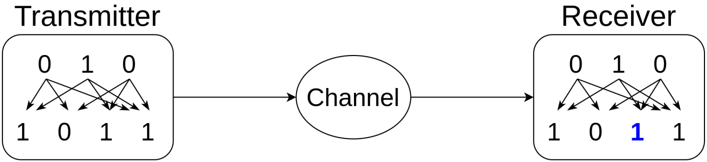

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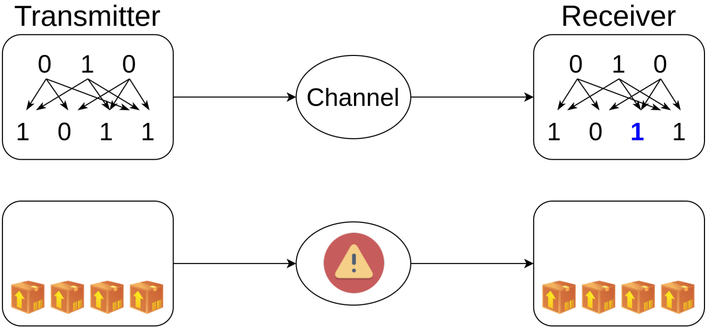

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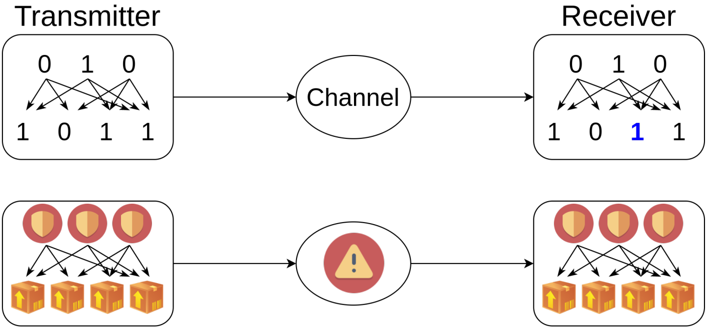

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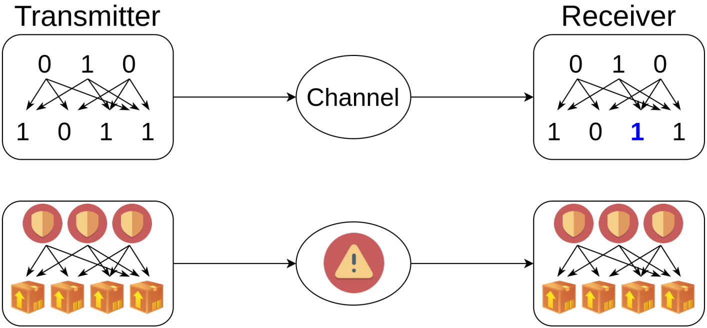

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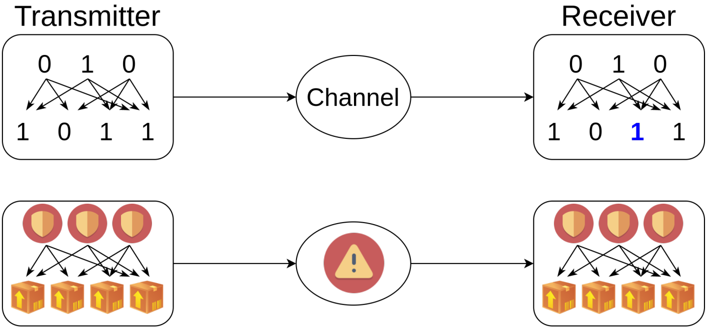

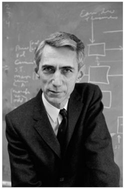

Channel Capacity:
Given channel condition, the maximum rate of information

Evolution of Digital Communications

- How to achieve the channel capacity?
- Various channel coding algorithms emerged (e.g. LDPC, Turbo).
- Polar codes provably achieve the channel capacity.
- They are involved as a coding scheme in 5G standard.

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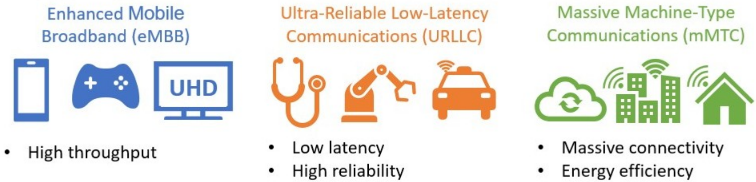
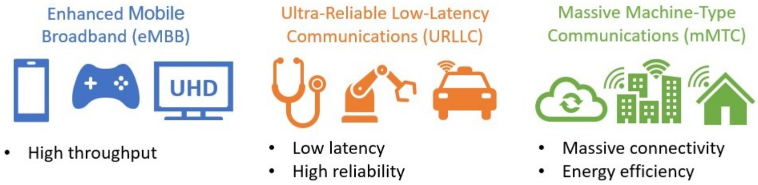
5G Use Cases



- 5G prioritizes various targets based on the use case.
- Polar codes are involved in 5G eMBB control channel.
- Currently, polar codes are considerable candidates for other use cases.
- Fast, practical, energy-efficient polar decoders are essential.

5G Use Cases



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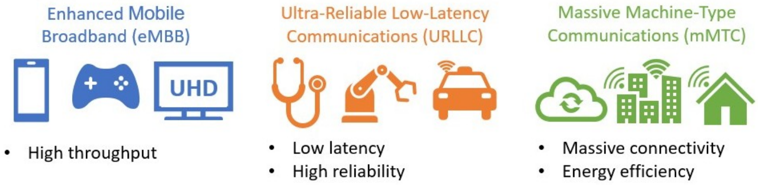

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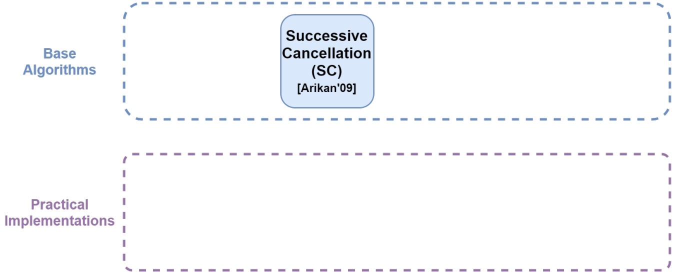
An Overview of Polar Decoders

Base
Algorithms

Practical
Implementations

An Overview of Polar Decoders



Successive Cancellation (SC) Decoding *

- ✓ Simple decoding
- ✗ Mediocre performance at practical lengths
- ✗ Sequential, long latency

* E. Arikan, "Channel Polarization: A Method for Constructing Capacity-Achieving Codes for Symmetric Binary-Input Memoryless Channels," in IEEE Tran. Inf. Theory, vol. 55, no. 7, pp. 3051-3073, July 2009.

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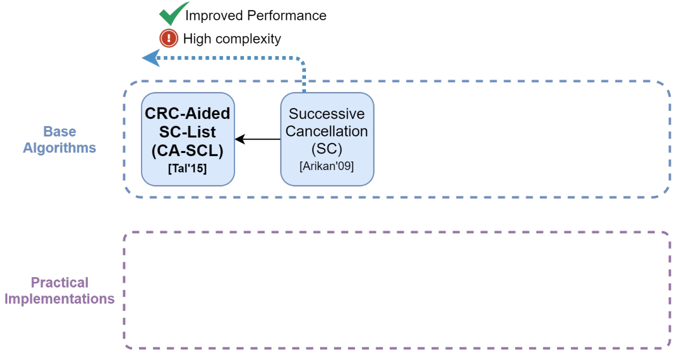


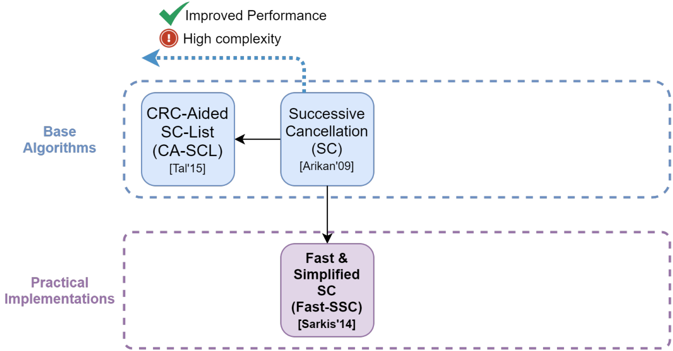
SC-List (SCL) Decoding *

✓ Improved error-correction performance

✗ Increased complexity

* I. Tal and A. Vardy, "List Decoding of Polar Codes," in IEEE TIT, May 2015.

An Overview of Polar Decoders



Fast-SSC Decoding *

✓ $\approx 10\times$ less latency

- No error correction performance degradation

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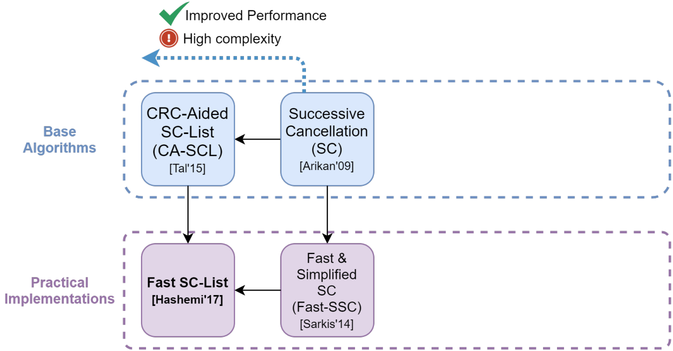
* G. Sarkis et al., "Fast Polar Decoders: Algorithm and Implementation," in IEEE JSAC, May 2014.

An Overview of Polar Decoders

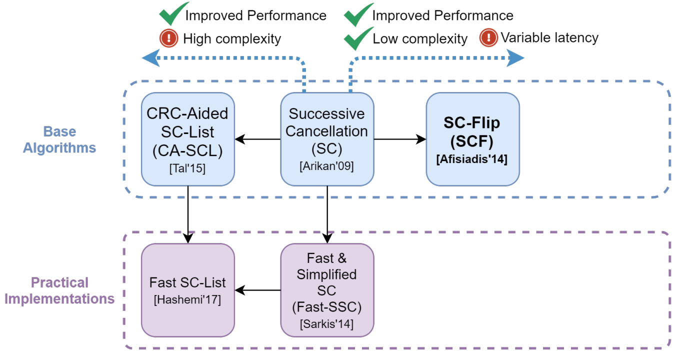


Fast-SC-List Decoding *

- ✓ Latency reduced further
- ✗ Very high complexity

* S. A. Hashemi et al. "Fast and Flexible Successive-Cancellation List Decoders for Polar Codes," in IEEE TSP, Nov. 2017.

An Overview of Polar Decoders



SC-Flip (SCF) Decoding *

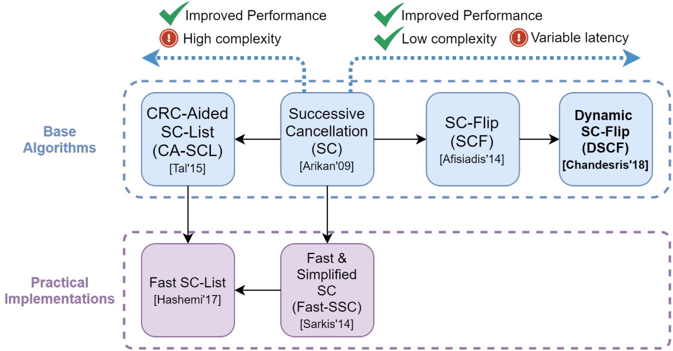
✓ Improved error-correction performance

✓ Low complexity

✗ Variable latency

* O. Afisiadis et al. "A low-complexity improved successive cancellation decoder for polar codes," 2014 48th Asilomar Conference, 2014.

An Overview of Polar Decoders

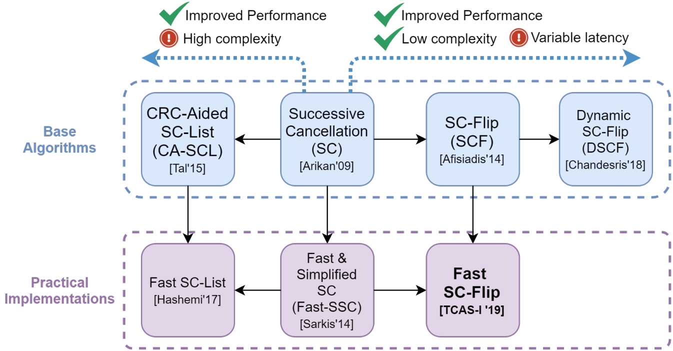


Dynamic SC-Flip (DSCF) Decoding *

- ✓ Improved error-correction performance
- ✗ Not practical due to complex computations

* L. Chandesris et al. "Dynamic-SCFlip Decoding of Polar Codes," in IEEE TCOM, June 2018.

An Overview of Polar Decoders



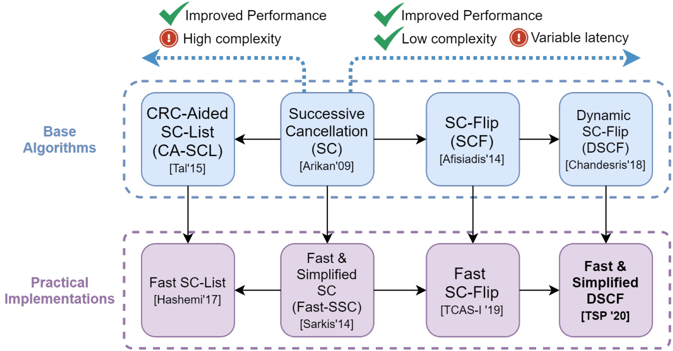
Fast SC-Flip Decoding *

✓ Introduced fast computations

✓ Energy-efficient implementation

* F. Ercan, et al. "Energy-Efficient Hardware Architectures for Fast Polar Decoders," in IEEE TCAS-I, Jan. 2020.

An Overview of Polar Decoders

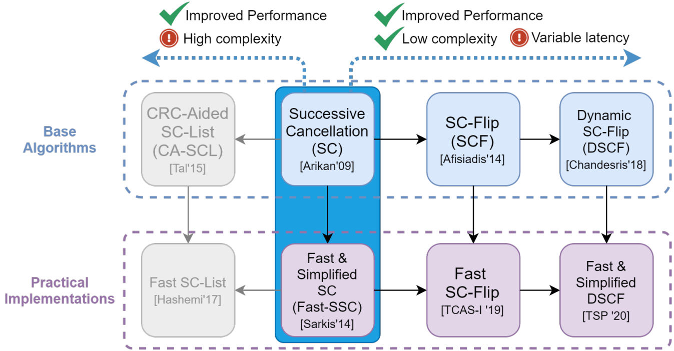


Practical Dynamic SC-Flip Decoding *

- ✓ Replaced complex computations with simple approximations
- ✓ Introduced fast computations
- ✓ First hardware implementation

* F. Ercan et al. "Practical Dynamic SC-Flip Polar Decoders: Algorithm and Implementation," in IEEE TSP, 2020.

An Overview of Polar Decoders



Overview of This Talk

- Part I: Background on SC Decoding
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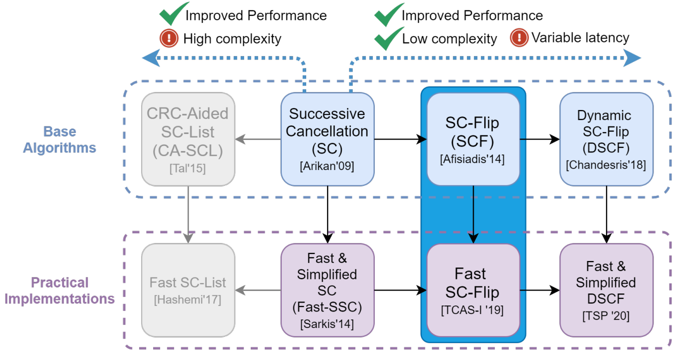

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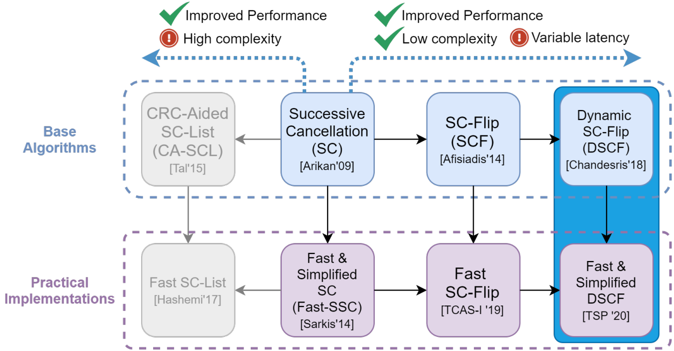


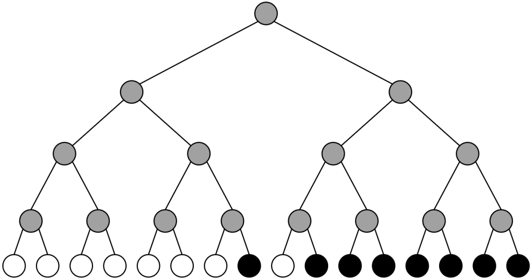
Overview of This Talk

- Part I: Background on SC Decoding
- Part II: Realizing the SC-Flip Algorithm in Hardware
- Part III: Making Dynamic SC-Flip Decoding Practical

Part I:
Preliminaries

SC Tree and Special Nodes

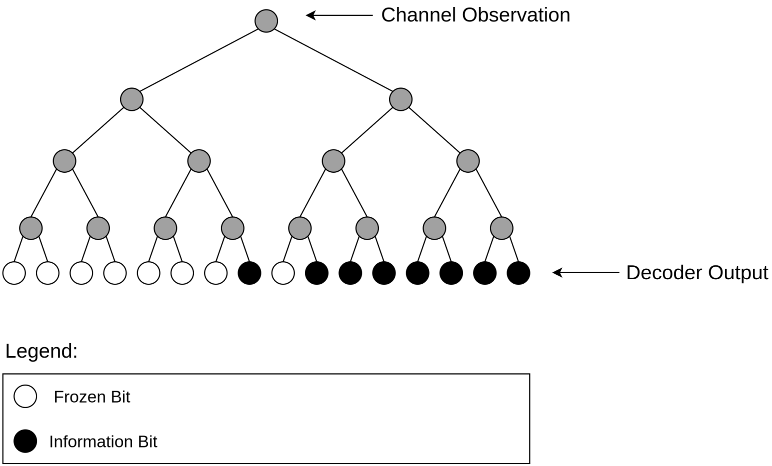
Example: PC(16,8)



Legend:

SC Tree and Special Nodes

Example: PC(16,8)



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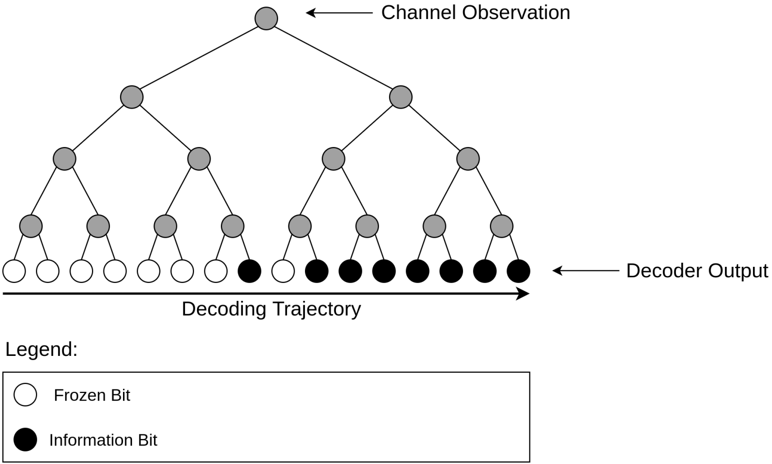

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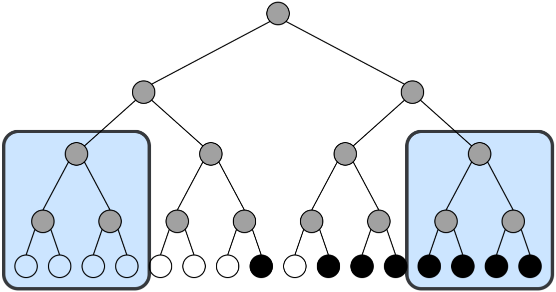

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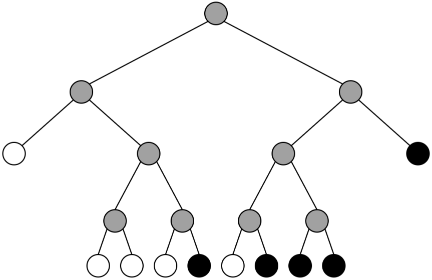

Legend:

Frozen Bit (Rate-0 Node)

Information Bit (Rate-1 Node)

SC Tree and Special Nodes

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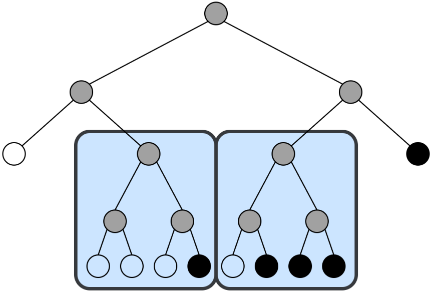
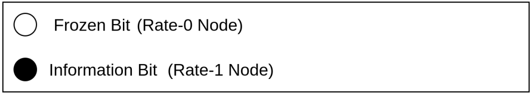


Legend:



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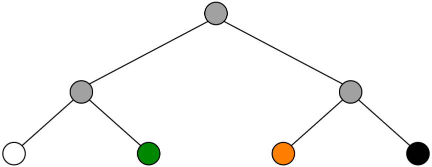

Legend:

- Frozen Bit (Rate-0 Node)
- Repetition Node
- Information Bit (Rate-1 Node)
- Single Parity Check Node

Fast Decoding v Energy Efficiency

- Energy = Power $\times$ Delay

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Table: SC Decoding, 65nm CMOS, PC(1024,512)

	SC[1]	Fast-SSC[2]
Power (mW)	51	160
Latency (μs)	12.7	0.6
Throughput (Mbps)	81	1719
Energy (pJ/bit)	1262	188

* Normalized for 65 nm CMOS.

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Power (mW)	75.3	119.7
Latency (μs)	1.71	0.43
Throughput (Mbps)	300	1201
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- Fast decoding: Huge gains in latency $>$ Penalty in power
- Motivation: Even more energy efficient with SCF
  - All while being competitive in error correction performance & T/P!

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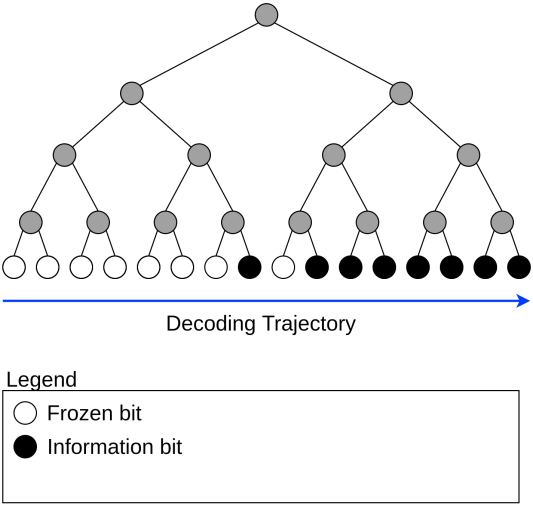
Part II:
Realizing the SC-Flip Algorithm

SC-Flip (SCF) Decoding



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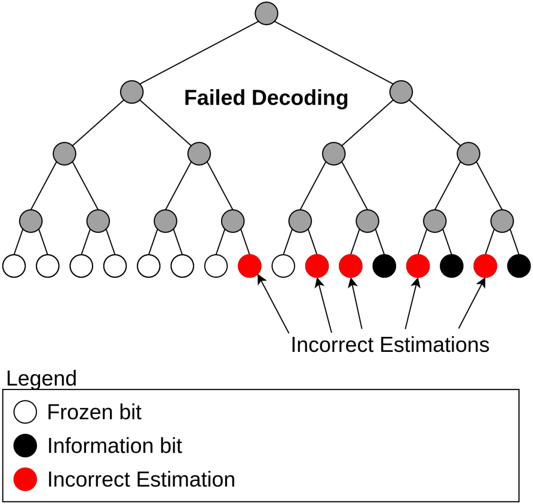

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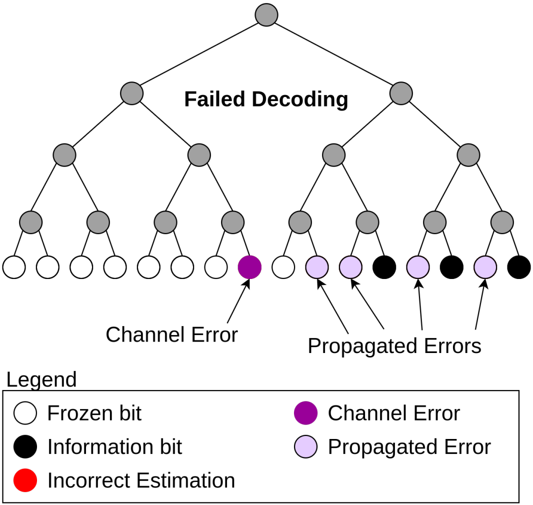

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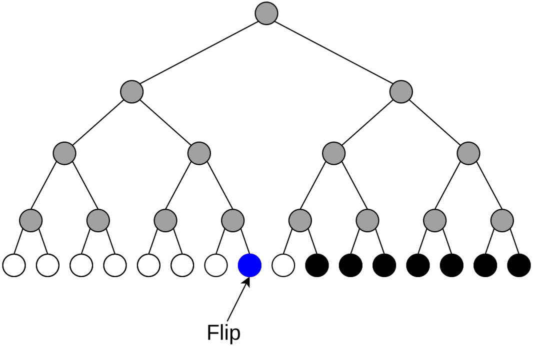

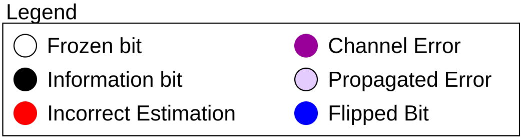

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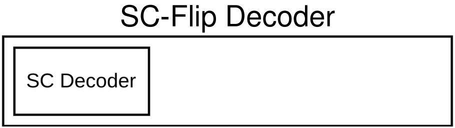
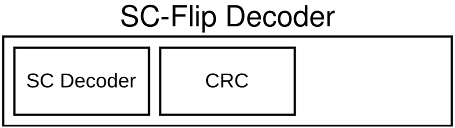
Components of SC-Flip Algorithm



- SC decoder
- An outer Cyclic Redundancy Check (CRC) decoder
  - To tell if a decoding attempt fails
- A sorter for bit-flipping indices
  - To sort them w.r.t. their reliability metric
  - Reliability metric: Log-likelihood ratio (LLR) value at each index

Components of SC-Flip Algorithm



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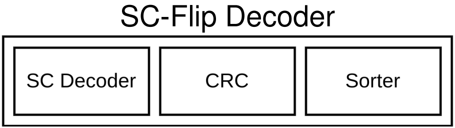

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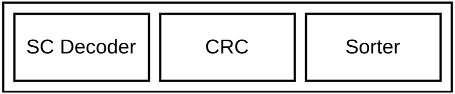
Previous Works on Fast SCF

SC-Flip Decoder



- Implementing fast nodes for SCF was proposed before [1],[2]
  - High sorting complexity
    - *i.e.* up to $n!$ bit-flipping candidates are evaluated in a node of size n
- No hardware architecture

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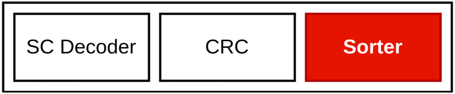

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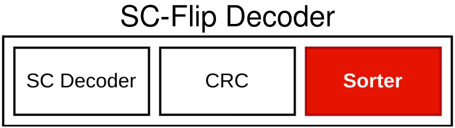

- Implementing fast nodes for SCF was proposed before [1],[2]
    - High sorting complexity
        - *i.e.* up to $n!$ bit-flipping candidates are evaluated in a node of size n
- No hardware architecture

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Our Work on Fast-SCF Decoding

Fast-SSC	CRC	Sorter

- An energy-efficient Fast-SSC architecture, to be used by Fast-SCF
    - Introduced resource sharing for merged operations
    - Reduced the overall memory requirement for soft and hard decision memories
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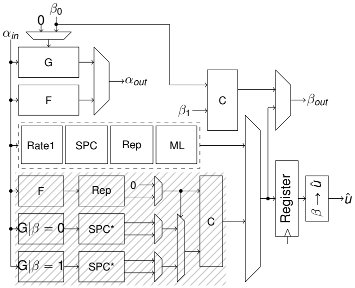

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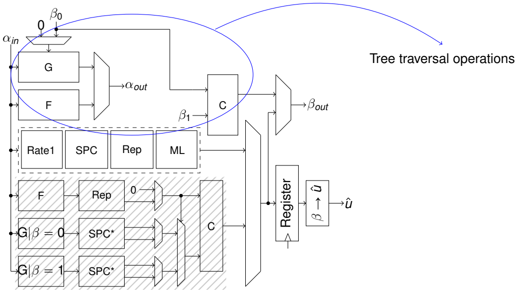

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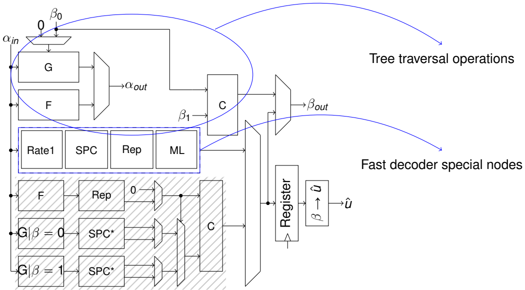

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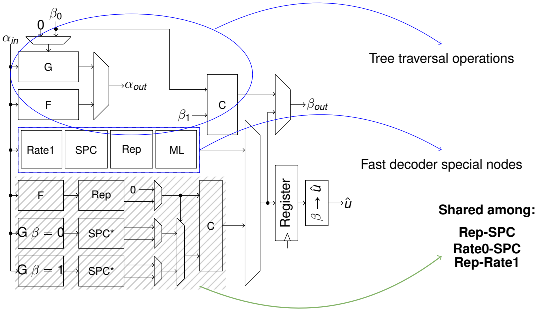

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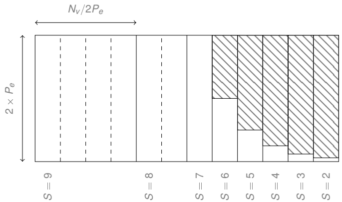

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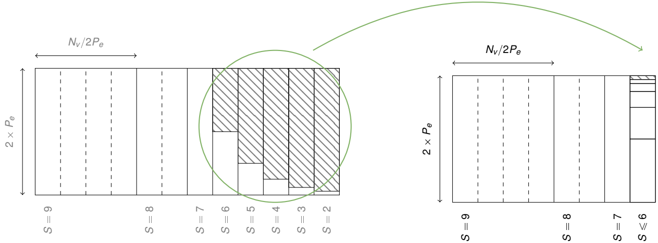

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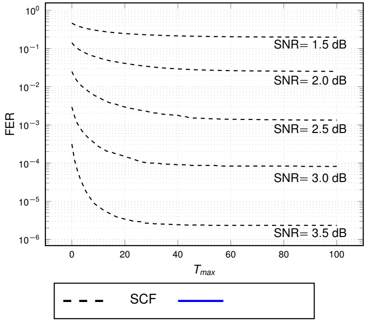

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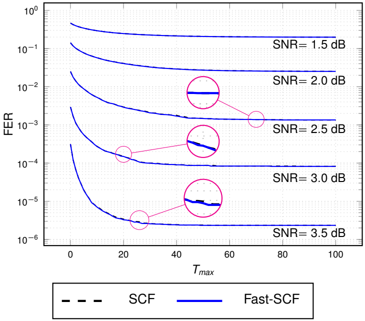

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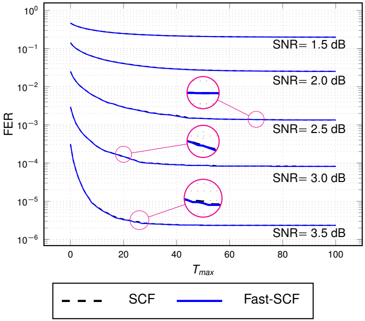

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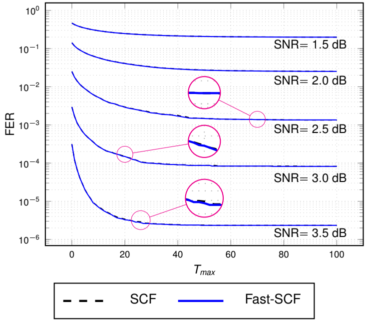

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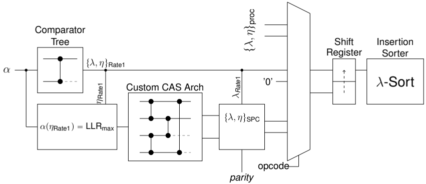

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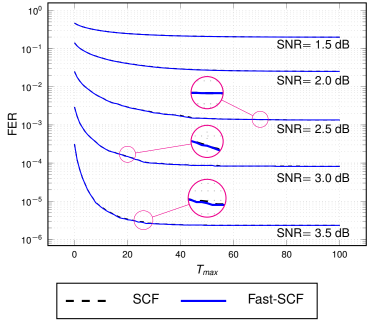

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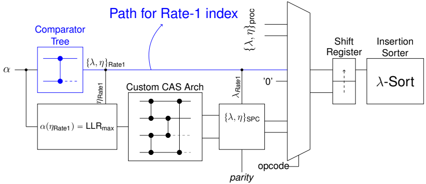

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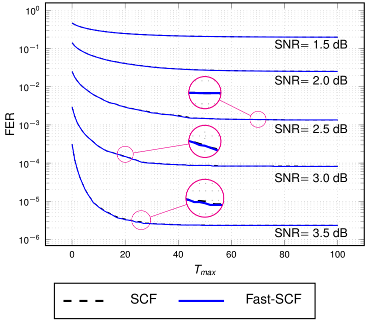

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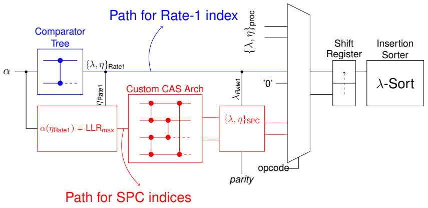

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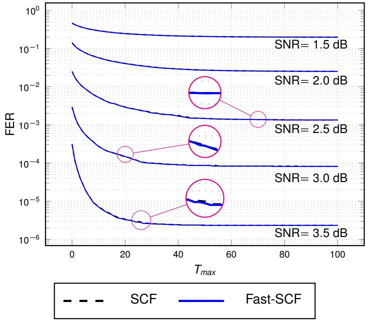

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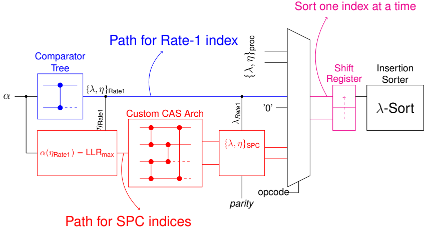

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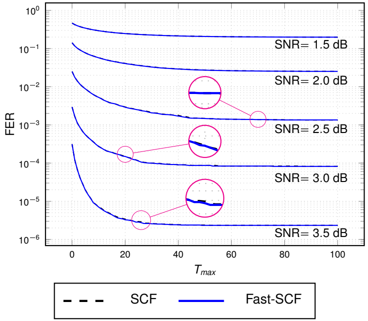

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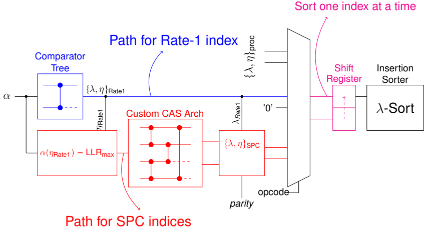

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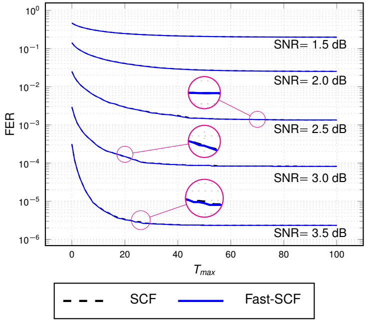

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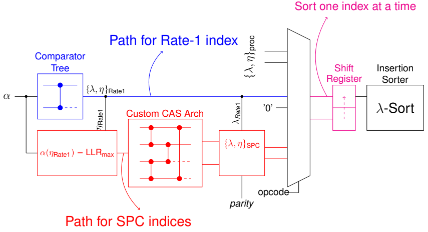
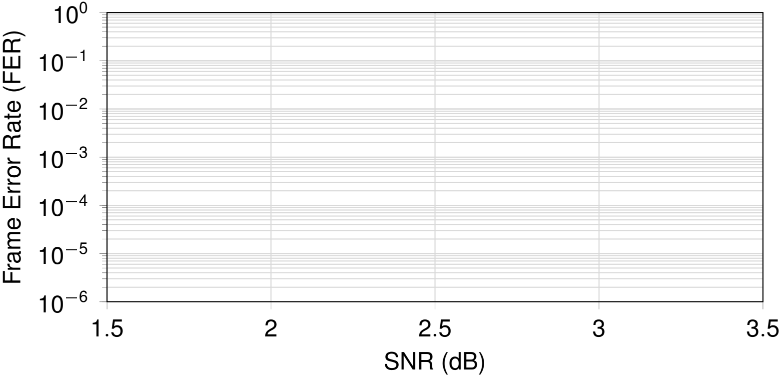


- Implemented a highly parallelized CRC datapath to support fast decoding
- Putting it altogether: An energy-efficient Fast-SCF polar decoder architecture

Simulation Results: Fast-SCF Decoding

5G $PC(1024, 512)$, 11-bit 5G CRC, $T_{max} = 20$



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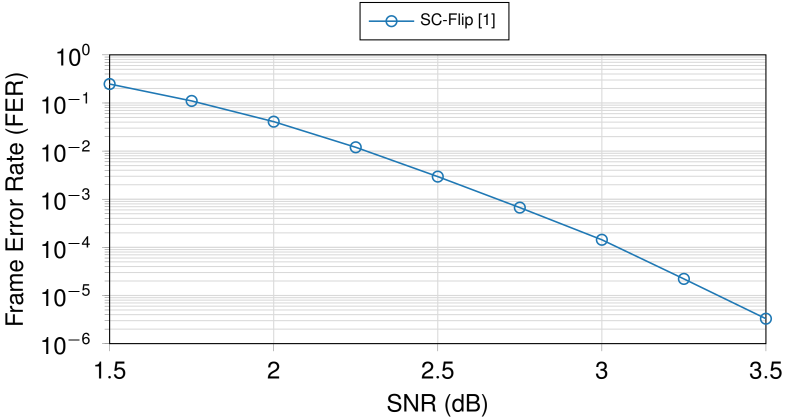

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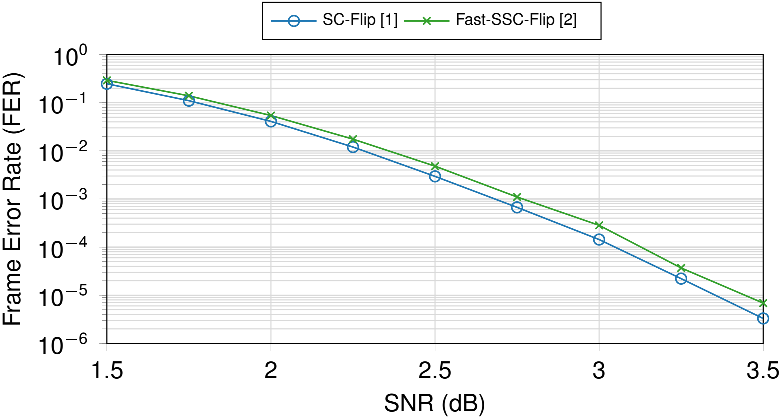

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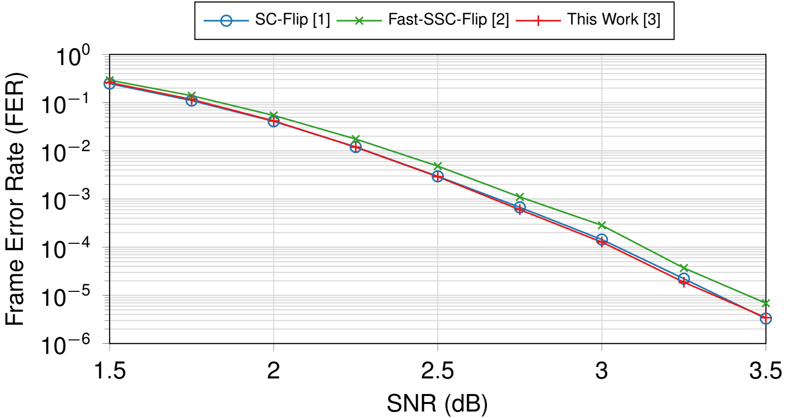

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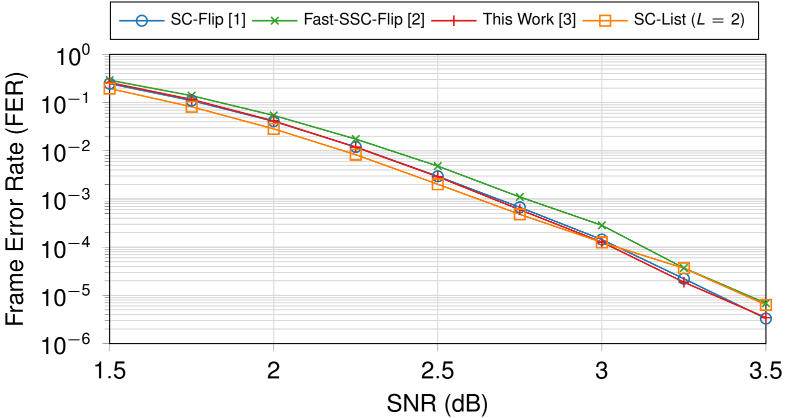

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Implementation Results: Fast-SCF Decoder

- TSMC 65nm CMOS technology
- $PC(512, 256)$

	SCL [1]	Fast-SSCL [2]	This Work[3]
Power (mW)	75.2	119.7	**57.4**
Latency (μs)	1.71	0.43	**0.33**
Worst Case Latency (μs)	1.71	**0.43**	6.93
Throughput (Mbps)	300	1201	**1552**
Area Efficiency (Gbps/mm^2)	1.36	2.85	**4.31**
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Part III:
Making Dynamic SC-Flip Decoding Practical

Dynamic SC-Flip (DSCF) Decoding

- A better metric that can distinguish channel errors from propagated errors.
- This gives an opportunity to tackle more than one channel error.
- Error correction performance is greatly improved.
- Metric computation is impractical:
  - $M(\mathcal{E}_\omega) = \sum_{j\in\mathcal{E}_\omega} |L^0[\mathcal{E}_{\omega-1}]_j| + \sum_{\substack{j\leqslant i_\omega \\ j\in\mathcal{A}}} \frac{1}{\alpha} \log\left(1 + \exp(-\alpha|L^0[\mathcal{E}_{\omega-1}]_j|)\right)$

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LLRs of flipping indices
(Same as SCF)

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LLRs of flipping indices
(Same as SCF)

Difficult part
$f_\alpha(|L|)$

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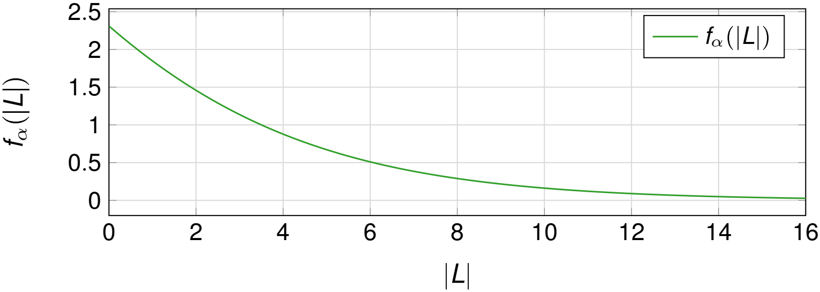

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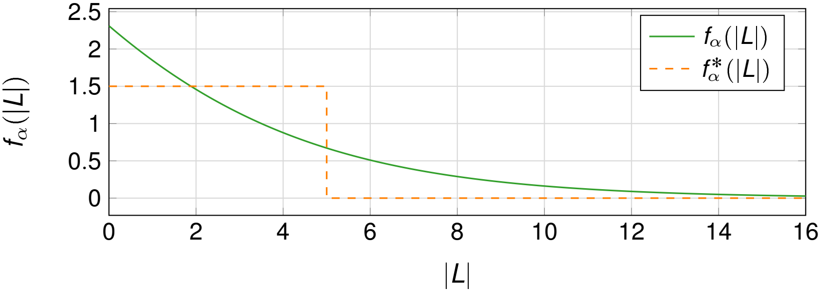

Replace $f_\alpha(x)$ with $f^*_\alpha(x) = \begin{cases} \frac{3}{2}, & \text{if } |x| \leqslant 5 \\ 0, & \text{otherwise.} \end{cases}$

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Towards Practical DSCF Decoding

Idea: Reformulate the simplified metric to be used in special nodes.
Recall the original DSCF metric:

$$M(\mathcal{E}_\omega) = \sum_{j \in \mathcal{E}_\omega} |L^0[\mathcal{E}_{\omega-1}]_j| + \sum_{\substack{j \leqslant i_\omega \\ j \in \mathcal{A}}} f_\alpha(|L^0[\mathcal{E}_{\omega-1}]_j|)$$

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Let us split it as follows:

$$M_\alpha(\mathcal{E}_\omega) = |L^0[\mathcal{E}_{\omega-1}]_{i_\omega}| + \sum_{j \in \mathcal{E}_{\omega-1}} |L^0[\mathcal{E}_{\omega-1}]_j| + \sum_{\substack{j \leqslant i_\omega \\ j \in \mathcal{A}}} f_\alpha(|L^0[\mathcal{E}_{\omega-1}]_j|).$$

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Let us split it as follows:

$$M_\alpha(\mathcal{E}_\omega) = \underbrace{|L^0[\mathcal{E}_{\omega-1}]_{i_\omega}|}_{M_1(L)} + \underbrace{\sum_{j \in \mathcal{E}_{\omega-1}} |L^0[\mathcal{E}_{\omega-1}]_j| + \sum_{\substack{j \leqslant i_\omega \\ j \in \mathcal{A}}} f_\alpha(|L^0[\mathcal{E}_{\omega-1}]_j|)}_{M_2(L)}.$$

- $M_1(L)$ is the *instantaneous component* obtained from the node, on the spot.
- $M_2(L)$ is the *accummulative component*, formed over the course of the decoding.

Incorporation of Special Nodes into DSCF

$$M(L) = M_1(L) + M_2(L).$$

- $M_1(L)$ is directly obtained from the LLR magnitude of the index.
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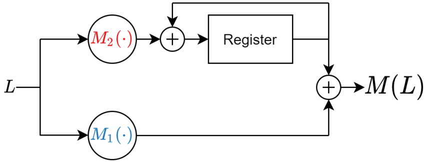

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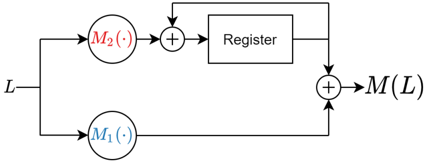

- **Main idea:** Obtain L from the special nodes.

More on Practical Fast-DSCF Decoding

- Algorithm-level improvements:
  - Performed a mathematical study to minimize the sorting complexity
- Hardware-level simplifications:
  - Normalized metric computation to avoid saturation
  - Custom sorter architecture to minimize delay
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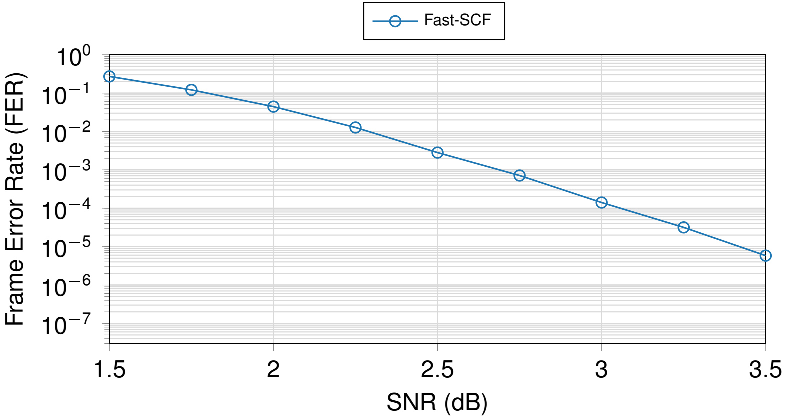
Simulation Results - Fast-DSCF Decoding

- 5G $PC(1024, 512)$, 16-bit 5G CRC, $T_{\max} = 400$.



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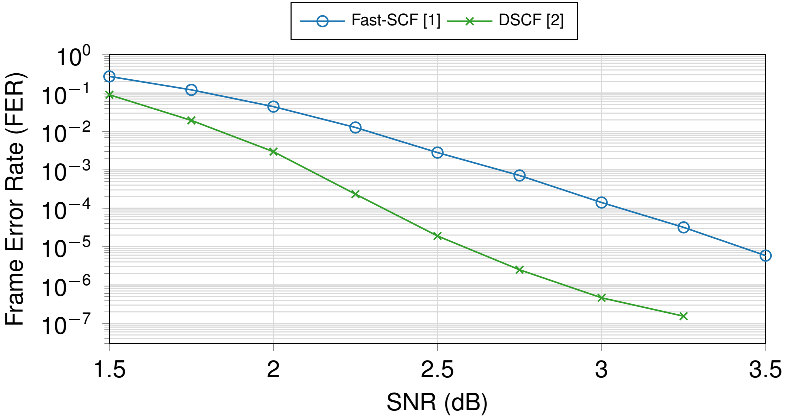

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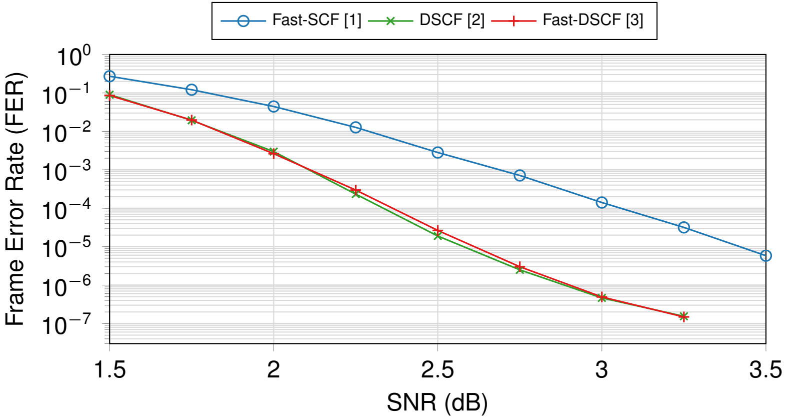

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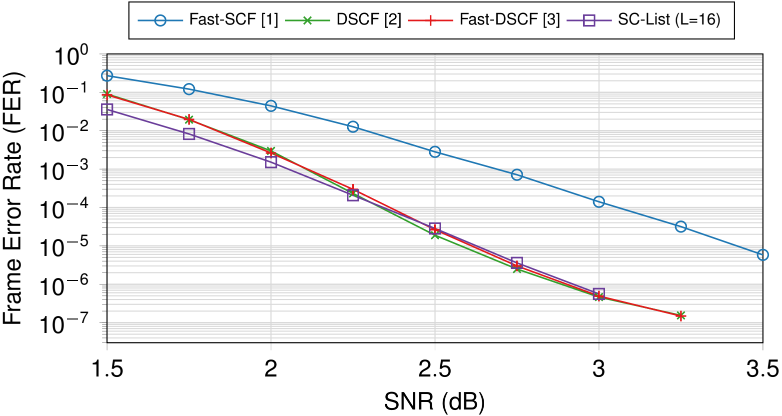

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Implementation Results: Fast-DSCF Decoder

- TSMC 65nm CMOS technology
- $PC(1024, 512)$

	SC-List [1]	SC-List [2]	This Work[3]
Frequency (MHz)	676	911	410
Area (mm^2)	4.21	3.90	**0.55**
Latency (μs)	**0.76**	1.60	1.11
Worst Case Latency (μs)	**0.76**	1.60	447
Average Throughput (Mbps)	**1340**	637	935
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