Energy-Efficient Polar Decoders for 5G and Beyond

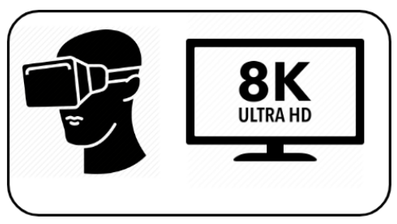
McGill University

Furkan Ercan*, Thibaud Tonnellier, Warren J. Gross

ISP Integrated Systems for Information Processing

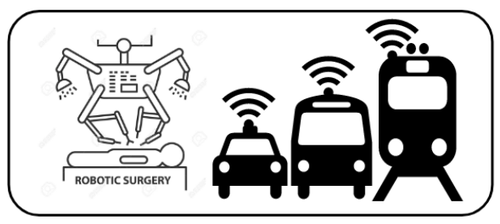
The three main 5G use cases

Enhanced Mobile Broadband (**eMBB**)



High Throughput

Ultra-Reliable Low-Latency Communications (**URLLC**)



Low Latency
High Reliability

Massive Machine-Type Communications (**mMTC**)

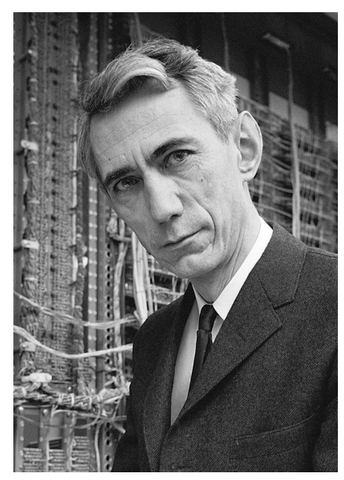
Massive Connectivity
Energy Efficiency

Channel Capacity

Claude E. Shannon

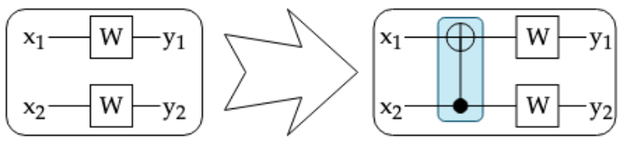
Known as the father of the information age

"There exists a maximum rate of information that can be transmitted reliably over a channel"

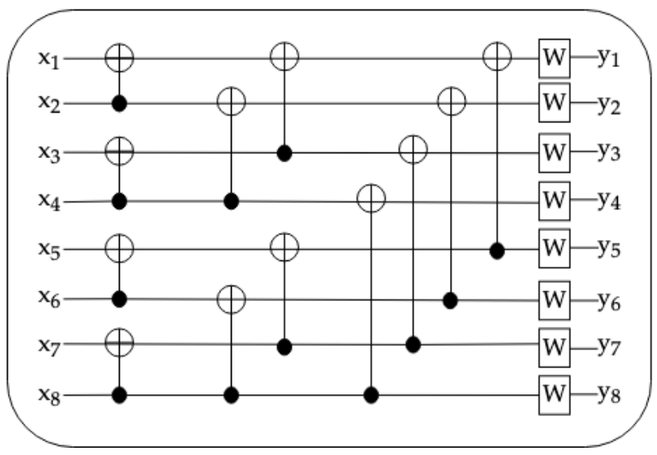


Polar Codes

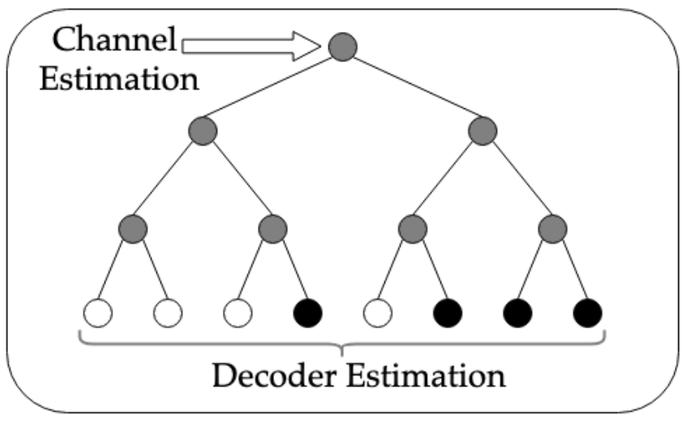
Channel polarization



Polar Code Encoding

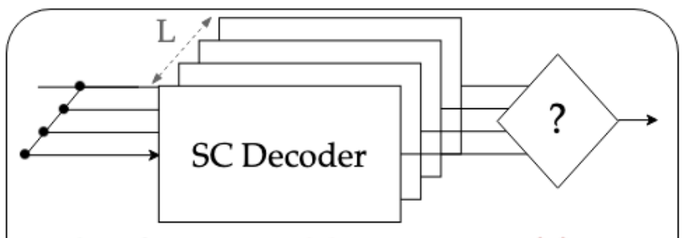


Successive Cancellation Decoding

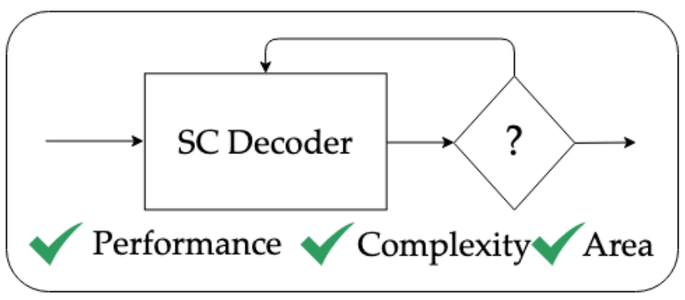


- ✓ Channel capacity @ code length → ∞
- ✓ Simple encoding / decoding
- ✗ Sequential decoding → slow
- ✗ Bad performance @ practical code lengths

SC-List (SCL) Decoding



SC-Flip (SCF) Decoding



What We Observed

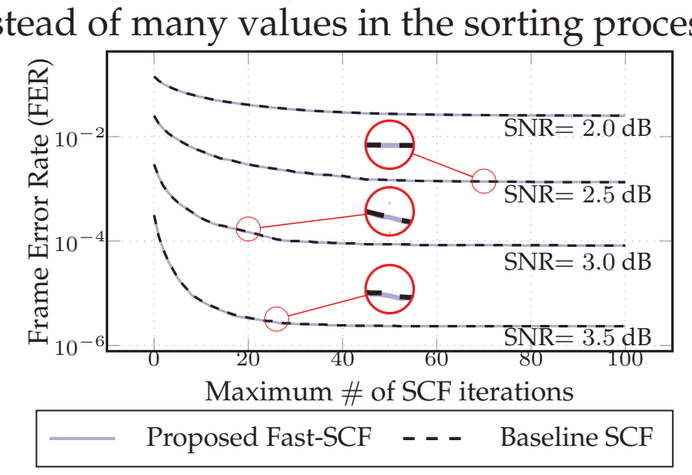
- Fast polar decoder architectures are more energy-efficient
- SCF decoding uses far less resources than SCL
- SCF has redundant operations/memories

What We Did

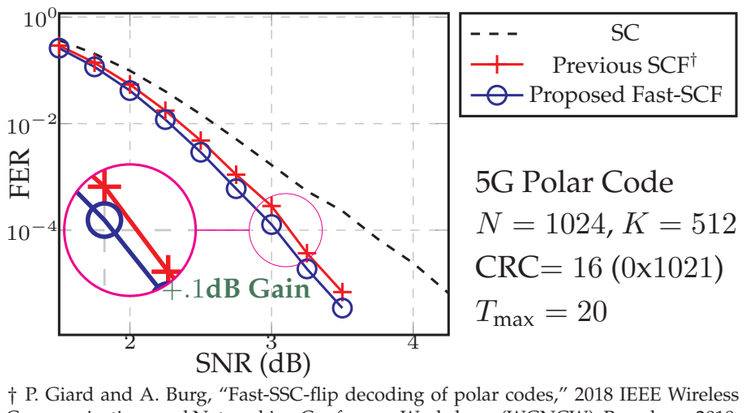
- An architecture that uses fast decoding for SCF **(Fast-SCF)**
- Eliminated the redundant operations and resources
- Reported architecture is the first for Fast-SCF algorithm

Algorithmic Improvements

Idea: Involve only the minimum value instead of many values in the sorting process



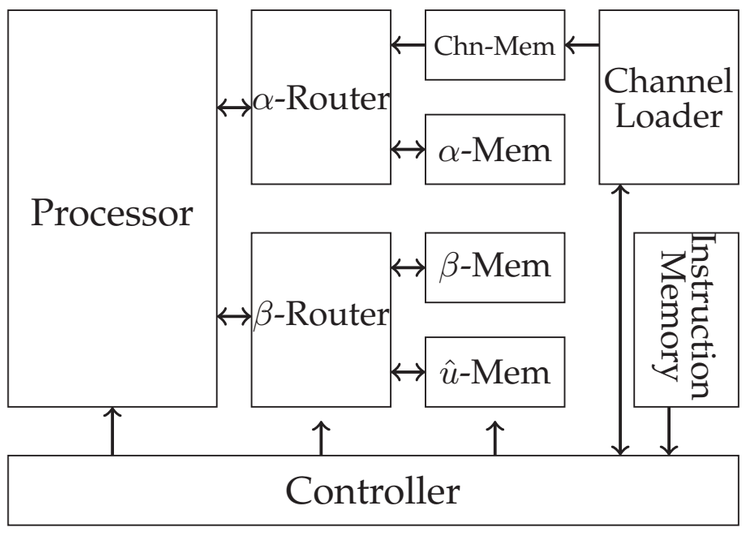
Decoding Performance



5G Polar Code
$N = 1024, K = 512$
CRC= 16 (0x1021)
$T_{max} = 20$

† P. Giard and A. Burg, "Fast-SSC-flip decoding of polar codes," 2018 IEEE Wireless Communications and Networking Conference Workshops (WCNCW), Barcelona, 2018, pp. 73-77.

Fast-SCF Architecture



Sorter Architecture

- Main beneficiary of the algorithmic improvements
- Then: 982 sorter elements in 28 stages
- Now: 228 sorter elements in 18 stages

Beta Memory

- Condensed utilization allows for 50% reduction at zero cost

Processor

- Increased resource sharing

Results

→ TSMC 65nm CMOS technology

→ Post-synthesis simulations

→ Real activity for accurate power

Using $PC(1024, 512)$

	Fast-SCF	SCF*
Power (mW)	83.44	**51.30**
Area (mm^2)	0.56	N/A
Latency (μs)	**14.2**	266.2
Throughput (Mbps)	**1511**	81
Energy (pJ/bit)	**110.4**	1270

*Giard et al. "PolarBear: A 28-nm FD-SOI ASIC for Decoding of Polar Codes," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 7, no. 4, pp. 616-629, Dec. 2017.

Using $PC(512, 256)$

	Fast-SCF	Fast-SSCL**
Power (mW)	**57.42**	119.68
Area (mm^2)	**0.36**	0.42
Latency (μs)	6.93	0.43
Throughput (Mbps)	**1552**	1201
Energy (pJ/bit)	**74.0**	199.3

**Hashemi et al. "Fast and Flexible Successive-Cancellation List Decoders for Polar Codes," in IEEE Transactions on Signal Processing, vol. 65, no. 21, pp. 5756-5769, 1 Nov.1, 2017.