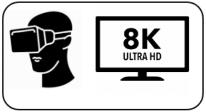
Energy-Efficient Polar Decoders for 5G and Beyond

Furkan Ercan
Quebec Engineering Competition 2020
Graduate Research Project Track

January 31, 2020

5G Use Cases

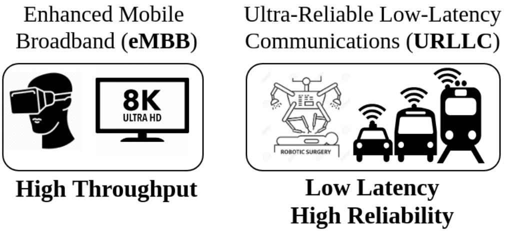
Enhanced Mobile Broadband (**eMBB**)



High Throughput

- High Throughput: Up to 20 Gbps

5G Use Cases



- High Throughput: Up to 20 Gbps
- Low Latency: Under 1 ms
- High Reliability: 1 in 10^9 error tolerance

5G Use Cases

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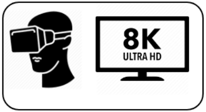
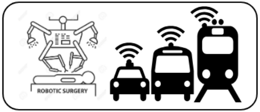


High Throughput

Ultra-Reliable Low-Latency Communications (**URLLC**)



Low Latency
High Reliability

Massive Machine-Type Communications (**mMTC**)

Massive Connectivity
Energy Efficiency

- High Throughput: Up to 20 Gbps
- Low Latency: Under 1 ms
- High Reliability: 1 in 10^9 error tolerance
- Massive Connectivity: 10^6 connected devices /km^2
- Energy Efficiency: Solutions are being formulated

Evolution of Communication Technologies

Definition

C. Shannon

1948

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LDPC Codes

R. Gallager

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Evolution of Communication Technologies

Definition	LDPC Codes	Turbo Codes	LDPC Codes	Polar Codes
				
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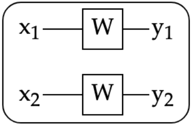
5G

Polar Codes

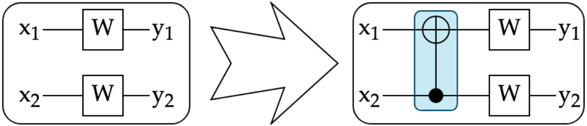
- Channel Polarization



- Polar Code Encoding

Polar Codes

- Channel Polarization



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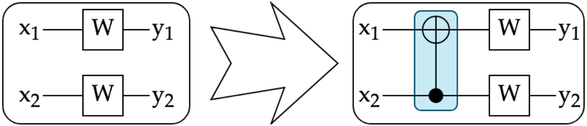

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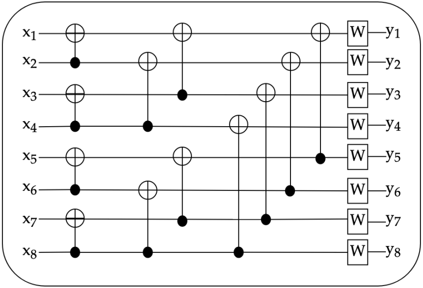
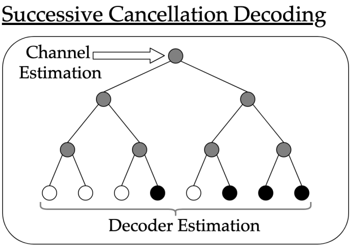
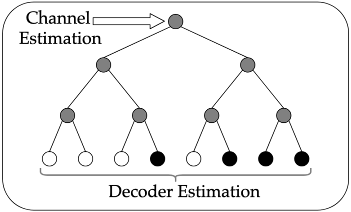


Decoding Polar Codes



Decoding Polar Codes

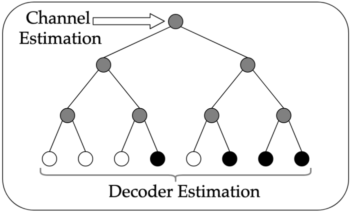
<u>Successive Cancellation Decoding</u>



✓ Channel capacity @ code length → ∞

Decoding Polar Codes

Successive Cancellation Decoding



- ✓ Channel capacity @ code length → ∞
- ✓ Simple encoding/decoding

Decoding Polar Codes

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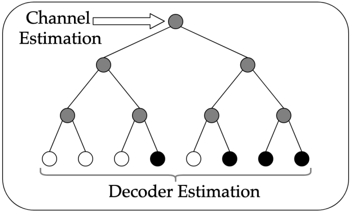

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Decoding Polar Codes

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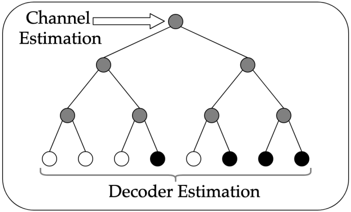

- ✓ Channel capacity @ code length $\rightarrow \infty$
- ✓ Simple encoding/decoding
- ✗ Sequential decoding $\rightarrow$ slow
- ✗ Bad performance @ practical code lengths

Decoding Polar Codes

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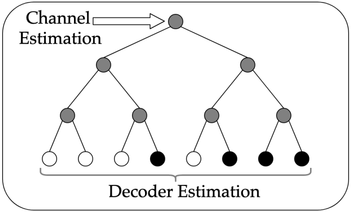

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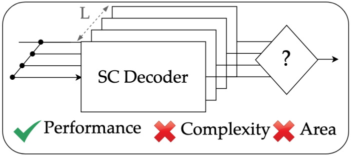
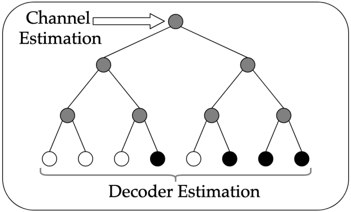
SC-List (SCL) Decoding



Decoding Polar Codes

Successive Cancellation Decoding



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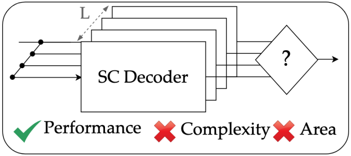
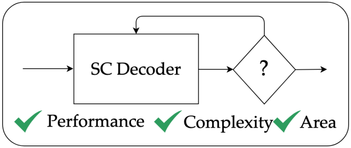
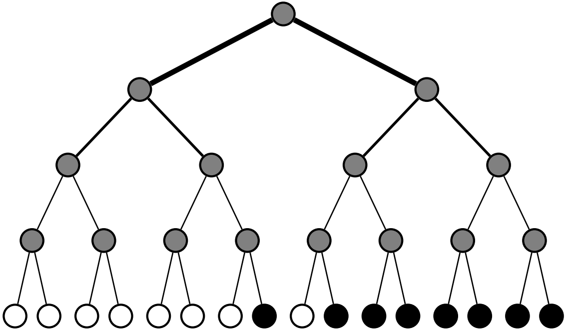


SC-Flip (SCF) Decoding

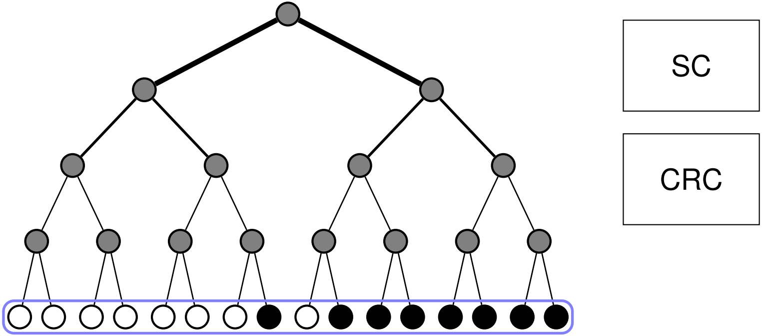


SCF Decoding



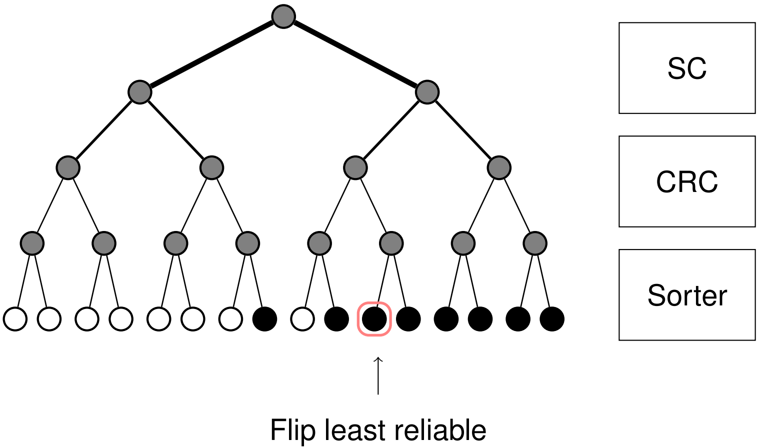
SC

SCF Decoding

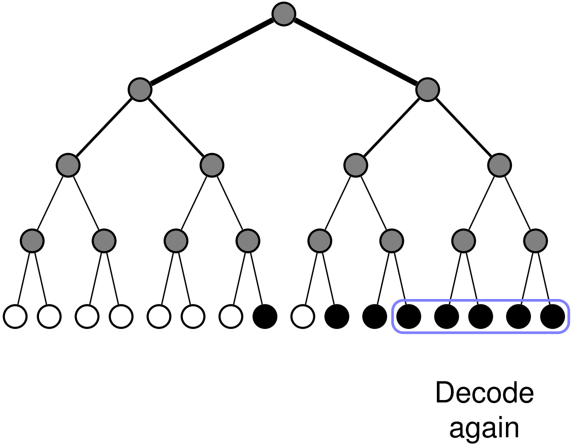


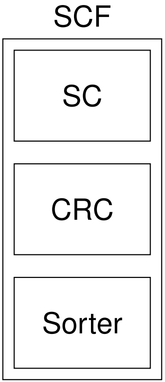
Failed decoding

SCF Decoding

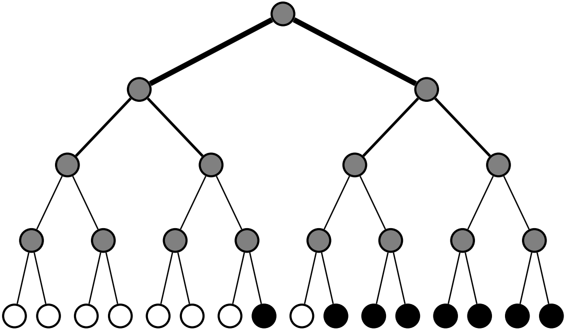


SCF Decoding





Fast Decoding Polar Codes



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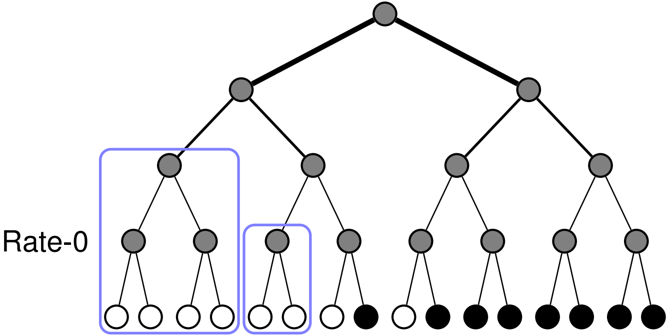

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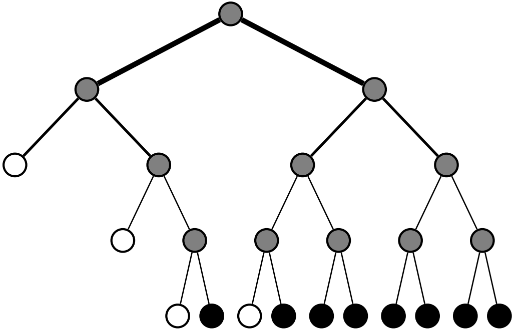

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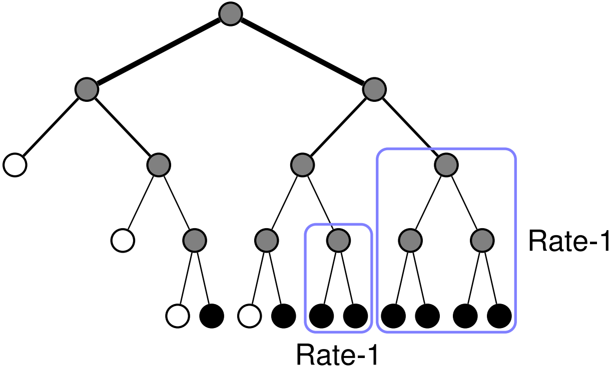

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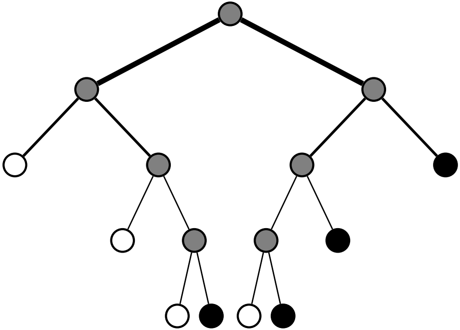

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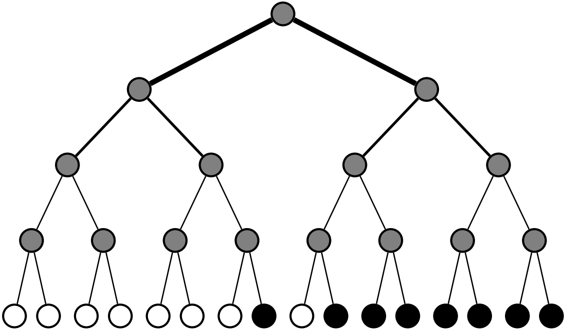

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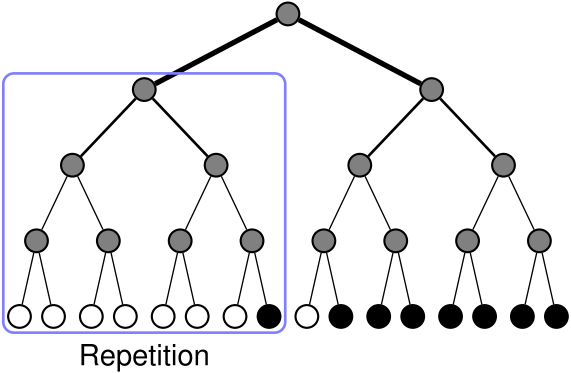

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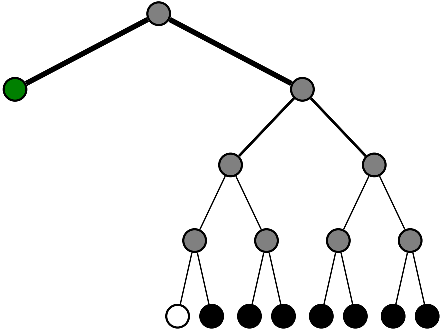

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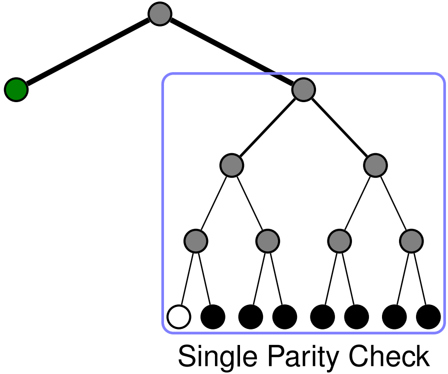

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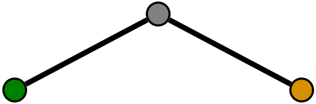

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Towards Energy-Efficient 5G Polar Decoders

- Energy Efficiency Essentials:
  - Less amount of:

Towards Energy-Efficient 5G Polar Decoders

- Energy Efficiency Essentials:
  - Less amount of: resources

Towards Energy-Efficient 5G Polar Decoders

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  - Less amount of: resources / computations

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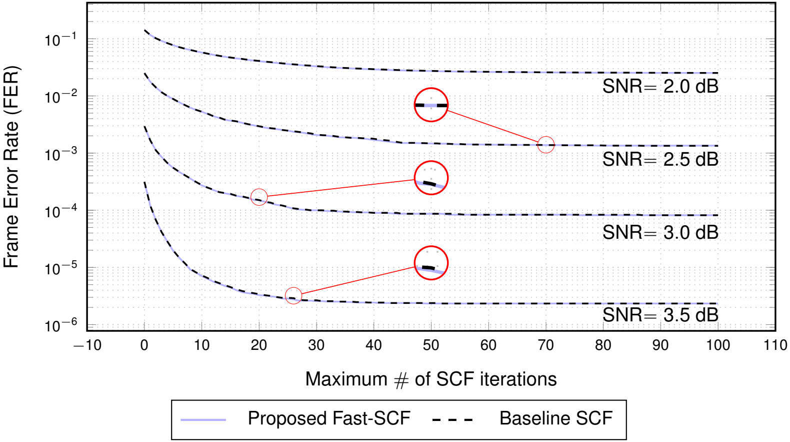
- What we did:
  - An architecture that is **fast** and uses **SCF** algorithm
  - Eliminated redundant computations in SCF
  - Reported architecture is the first of its kind

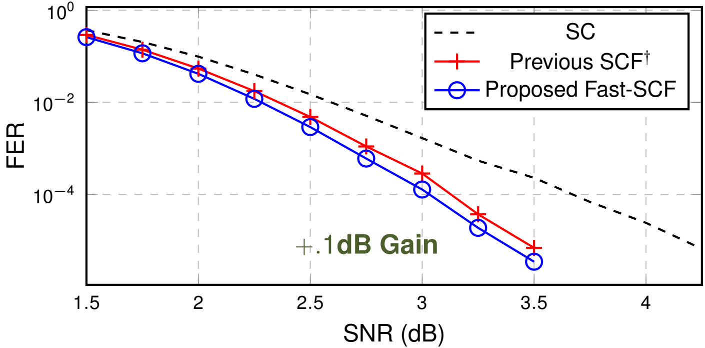
Eliminating Redundant Computations of SCF

- SCF typically sorts **hundreds of values** in the SC tree
- We scaled it down to **tens of them**



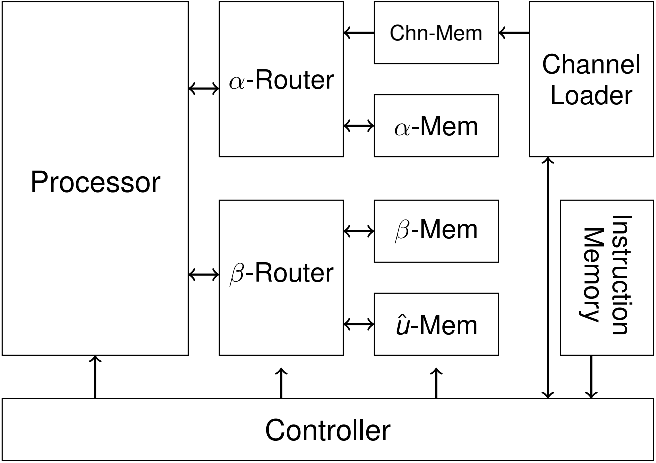
Decoding Performance

- 5G Polar Code
- $N = 1024$, $K = 512$
- CRC=16 (0x1021)
- $T_{\max} = 20$



P. Giard and A. Burg, "Fast-SSC-flip decoding of polar codes," 2018 IEEE WCNC Workshops, Barcelona, 2018, pp. 73-77.

Decoder Architecture



Architectural Improvements

- Sorter architecture: Main beneficiary of algorithmic improvements
  - What was: 982 elements in 28 stages
  - What is: 228 elements in 18 stages
- Beta memory: 5G sequence allows for 50% reduction at zero cost
- Processor: Introduced resource sharing to reduce power

Results-I

→ TSMC 65nm CMOS technology

→ Post-synthesis simulations

→ Real activity for accurate power

Using $PC(1024, 512)$:

	Fast-SCF	SCF*
Power (mW)	83.44	**51.30**
Area (mm^2)	0.56	N/A
Latency (μs)	**14.2**	266.2
Throughput (Mbps)	**1511**	81
Energy (pJ/bit)	**110.4**	1270

* Giard et al., "PolarBear: A 28-nm FD-SOI ASIC for Decoding of Polar Codes," in IEEE JETCAS, vol. 7, no. 4, Dec. 2017.

Results-II

→ TSMC 65nm CMOS technology

→ Post-synthesis simulations

→ Real activity for accurate power

Using $PC(512, 256)$:

	Fast-SCF	Fast-SSCL**
Power (mW)	**57.42**	119.68
Area (mm^2)	**0.36**	0.42
Latency (μs)	6.93	**0.43**
Throughput (Mbps)	**1552**	1201
Energy (pJ/bit)	**74.0**	199.3

**Hashemi et al. "Fast and Flexible Successive-Cancellation List Decoders for Polar Codes," in IEEE Transactions on Signal Processing, vol. 65, no. 21, pp. 5756-5769, 1 Nov.1, 2017.

Conclusion

- We have described a novel, energy-efficient 5G polar decoder architecture.
- Algorithmic improvements reduce sorter complexity.
- Architectural improvements reduce power and latency.
- Compared to the state-of-the-art decoders with equivalent decoding performance, proposed architecture is
  - 29% faster,
  - 51% more area-efficient,
  - 2.7$\times$ more energy-efficient.
- Proposed scheme is a favorable candidate for 5G mMTC platforms.

Reference

Energy-Efficient Hardware Architectures for Fast Polar Decoders

Furkan Ercan, *Student Member, IEEE*, Thibaud Tonnellier, and Warren J. Gross, *Senior Member, IEEE*

***Abstract*—Interest in polar codes has increased significantly upon their selection as a coding scheme for the 5th generation wireless communication standard (5G). While the research on polar code decoders mostly targets improved throughput, few implementations address energy consumption, which is critical for platforms that prioritize energy efficiency, such as massive machine-type communications (mMTC). In this work, we first propose a novel Fast-SSC decoder architecture that has novel architectural optimizations to reduce area, power, and energy consumption. Then, we extend our work to an energy-efficient implementation of the fast SC-Flip (SCF) decoder. We show that sorting a limited number of indices for extra decoding attempts is sufficient to practically match the performance of SCF, which enables employing a low-complexity sorter architecture. To our knowledge, the proposed SCF architecture is the first hardware realization of fast SCF decoding. Synthesis results targeting TSMC 65nm CMOS technology show that the proposed Fast-SSC decoder architecture is 18% more energy-efficient, has 14% less area and 30% less power consumption compared to state-of-the-art decoders in the literature. Compared to the state-of-the-art available SC-List (SCL) decoders that have equivalent error-correction performance, proposed Fast-SCF decoder is 29% faster while being 2.7× more energy-efficient and 51% more area-efficient.**

***Index Terms*—Polar codes, 5G, energy efficiency, Fast-SSC, SCFlip, wireless communications, hardware implementation.**

I. Introduction

POLAR codes have gained significant attention due to the fact that they have simple encoding/decoding algorithms and that they provably achieve channel capacity [1]. They have

decoding. Moreover, the sequential procedure of SC decoding is a limiting factor in decoding latency. SC-List (SCL) decoding [5] improves the error-correction performance at the cost of increased complexity [6]. On the other hand, SC-Flip (SCF) [7] decoding demonstrates improved error-correction compared to SC while keeping a computational complexity similar to that of SC at medium-to-high signal-to-noise ratios (SNRs). Nevertheless, SCF decoding comes with a variable decoding latency, which makes SCF unfavorable for applications that require deterministic latency.

Frozen bit patterns in the polar code sequence, called special nodes, were identified previously in [8]–[10] for SC decoding; customized decoding techniques for these special nodes yields in significantly improved throughput. Adaptation of these special nodes to SCL decoding was carried out in [11]–[13]. On the other hand, although applications of such special node decoding techniques were detailed for SCF in [14] and [15], no hardware implementation has been proposed previously.

While the research on polar code decoders mostly targets improved throughput, few implementations address energy consumption [16], which is critical for use cases that prioritize energy efficiency, such as massive machine-type communications (mMTC) [17]. While systematic polar codes exhibit an improved bit error rate (BER) compared to non-systematic polar codes [18], [19], the 5G standard considers non-systematic polar codes [20]. The broad focus of this

Thank you for your attention!

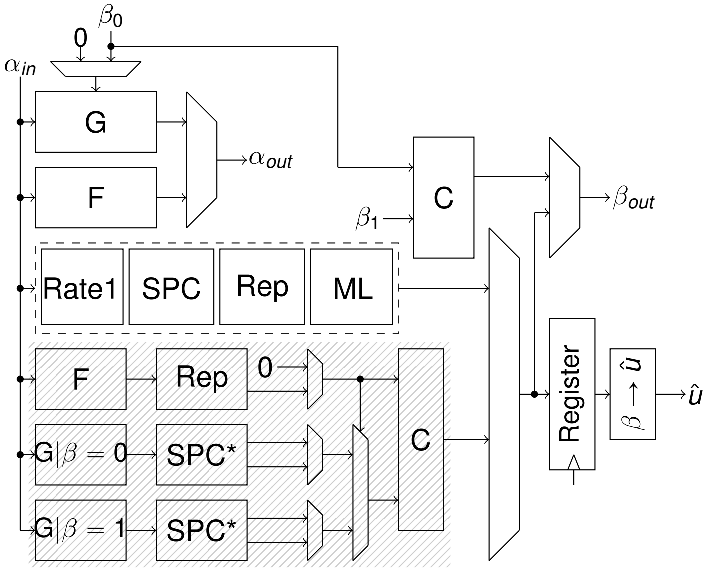
Backup

But Why Fast Decoding?

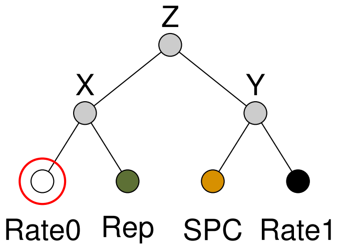
	SCL [1]	SSCL[2]	Fast-SSCL[3]
Power (mW)	75.27	98.91	119.68
Latency (μs)	1.71	0.85	0.43
Throughput (Mbps)	300	605	1201
Energy (pj/bit)	502	327	199

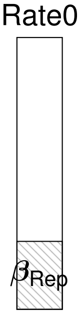
[1] Stimming et al., "LLR-Based Successive Cancellation List Decoding of Polar Codes," in IEEE TSP, vol. 63, no. 19, 2015.
[2] Hashemi et al.,"A Fast Polar Code List Decoder Architecture Based on Sphere Decoding," in IEEE TCAS-I, vol. 63, no. 12, 2016.
[3] Hashemi et al.,"Fast and Flexible Successive-Cancellation List Decoders for Polar Codes," in IEEE TSP, vol. 65, no. 21, 2017.

Processor Datapath



Partial Sum (β) Memory - Prior Art





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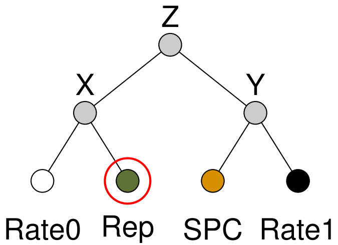

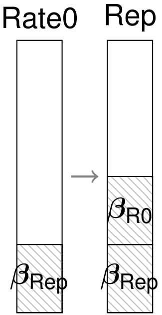

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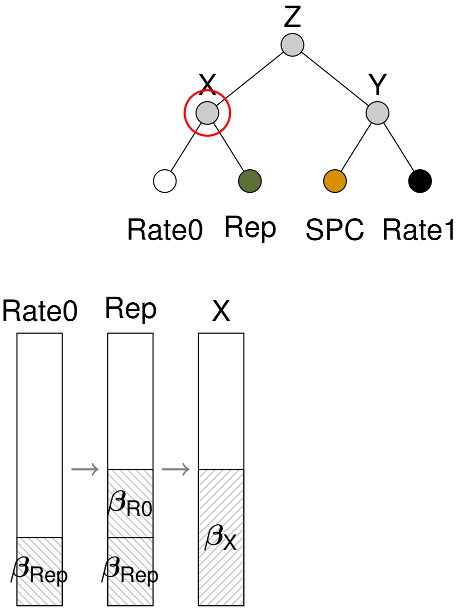

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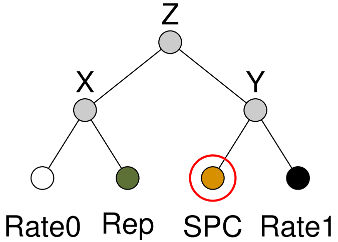

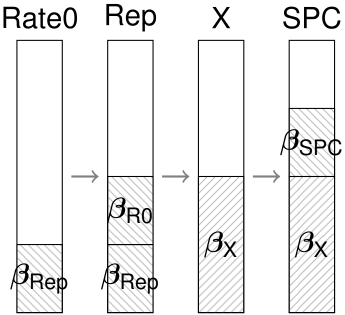

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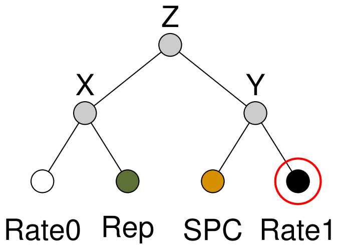

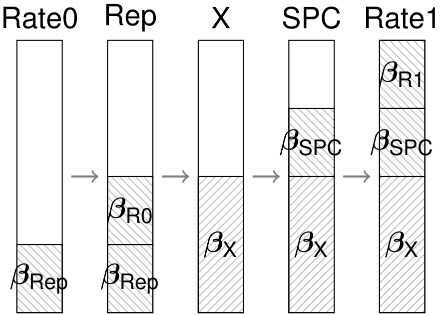

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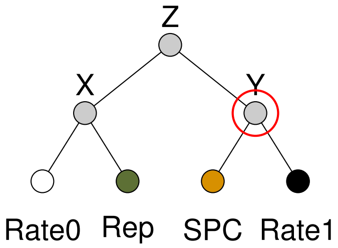

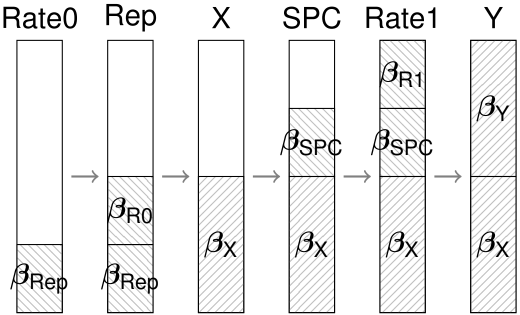

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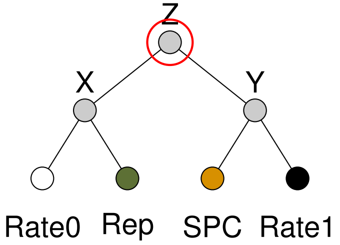

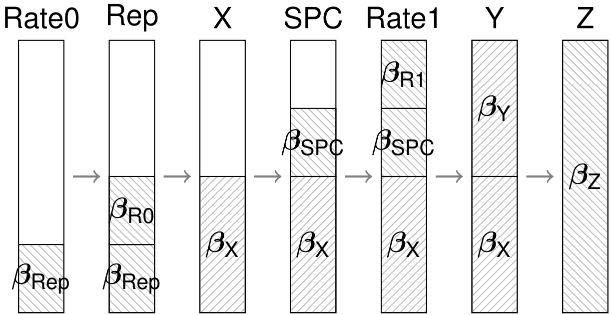

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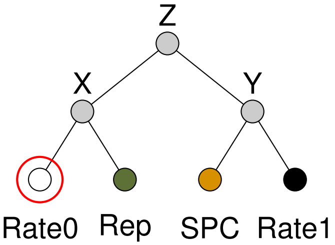

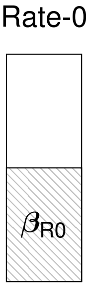

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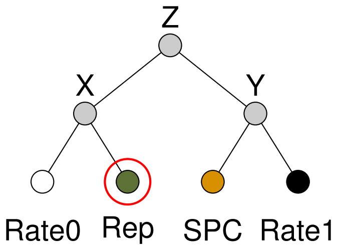

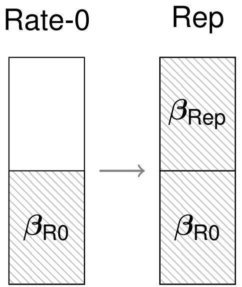

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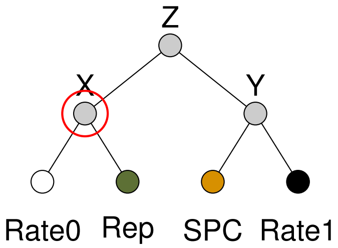

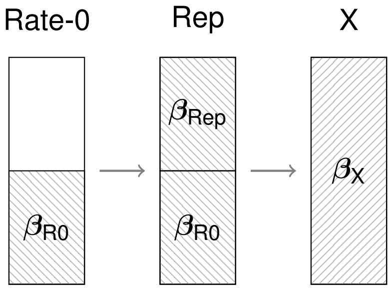

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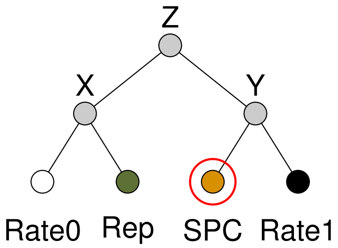

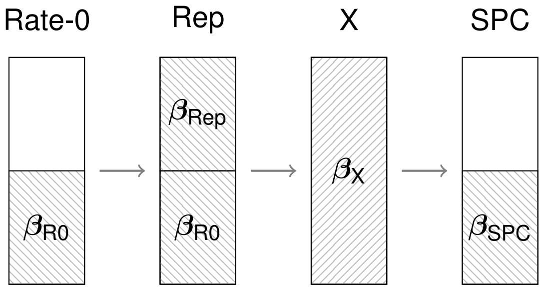

Partial Sum (β) Memory - Our Work